

COMPAL CONFIDENTIAL

MODEL NAME : PAL61
PCB NO : LA-6561P (DA80000JO10)
DAZ NO : DAZ0FI00100
BOM P/N : 43193131L01,46193131L03.

GPIO MAP: E3 Master GPIO Map10102010.xlsx

E3 MACALLAN 15.6" SG
rPGA Sandy Bridge +
FCBGA PCH Cougar Point-M

2011-01-12

REV : 1.0(A00)

www.aitech1.ru
@ : Nopop Component
CONN@ : Connector Component

MB Type	BOM P/N	
TPM EN/ TCM DIS	43193131L01 (R1)	1@ 3@
TPM DIS/ TCM EN	43193131L02 (R1)	2@ 4@
TPM DIS/ TCM DIS	43193131L03 (R1)	2@ 3@

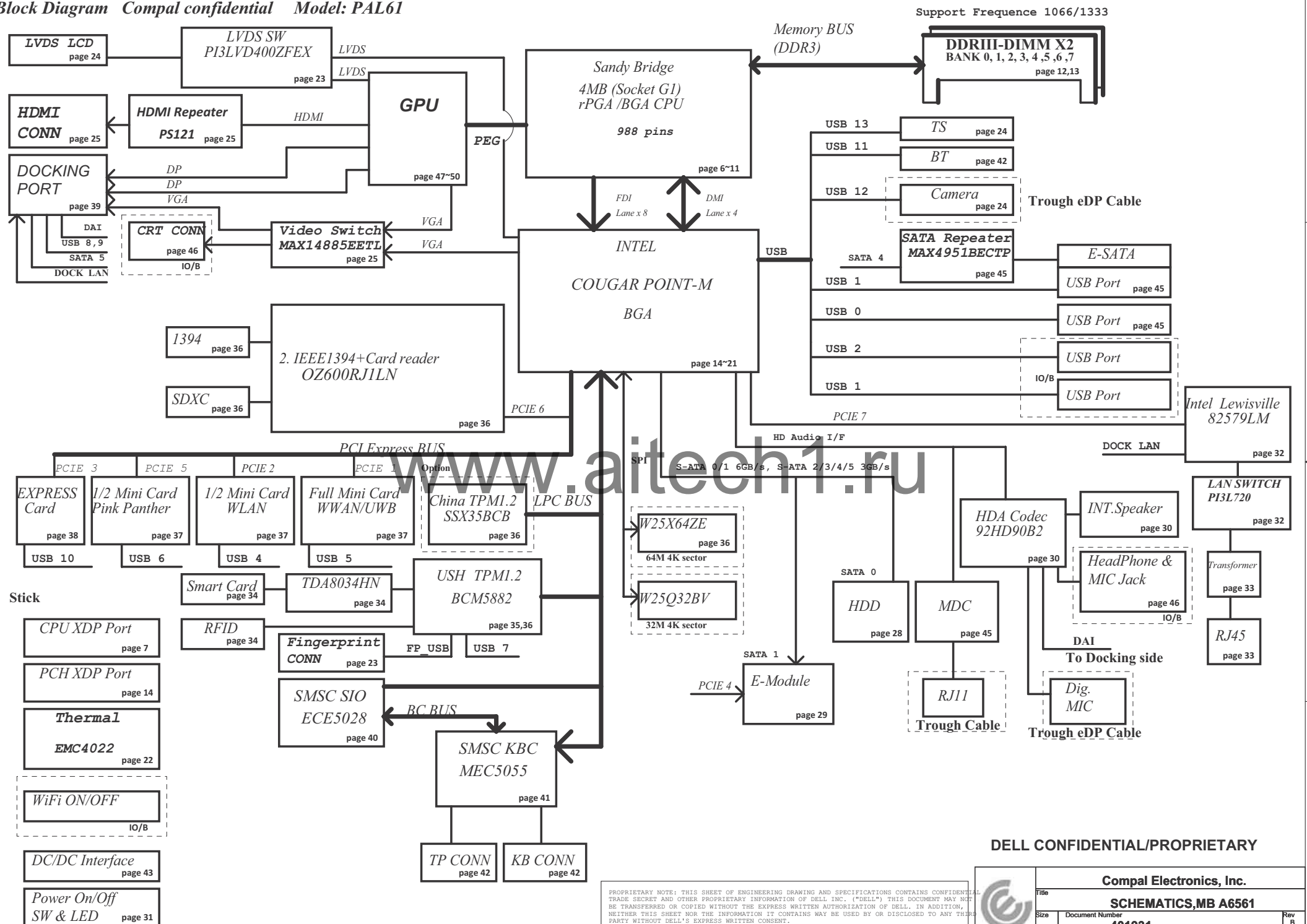
MB PCB	
Part Number	Description
DA800001700	PCB OFI LA-6561P REV0 M/B DSC

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Block Diagram *Compal confidential* **Model: PAL61**



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POWER STATES

Signal State	SLP S3#	SLP S4#	SLP S5#	S4 STATE#	SLP M#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M1	LOW	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M1	LOW	LOW	HIGH	LOW	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M1	LOW	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

power plane State	+15V_ALW +5V_ALW +3.3V_ALW_PCH +3.3V_RTC_LDO	+3.3V_SUS +1.5V_MEM	+5V_RUN +3.3V_RUN +1.8V_RUN +1.5V_RUN +0.75V_DDR_VTT +VCC_CORE +1.05V_RUN_VTT +1.05V_RUN	+3.3V_M +1.05V_M	+3.3V_M +1.05V_M (M-OFF)
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	ON	OFF
S5 S4/AC	ON	OFF	OFF	ON	OFF
S5 S4/AC don't exist	OFF	OFF	OFF	OFF	OFF

Enginner proposal (Unit : mil)						
Layer No.	Name	Dielectric Constant	Material		Thickness (Material SPEC.) Unit : mil	Thickness (Actuality) Unit : mil
			SolderMask		0.6	0.50
			Add Plating		1.3	1.40
1	Top		Copper foil		0.5oz	0.70
			Prepreg	1080LRC	2.80	2.67
2	GND		Copper foil		0.5oz	0.70
			Core	3mil H/1	3.00	3.00
3	Sig1		Copper foil		1.0oz	1.30
			Prepreg	7628HRC*2	17.06	15.10
4	Sig2		Copper foil		1.0oz	1.30
			Core	3mil 1/1	3.00	3.00
5	VCC		Copper foil		1.0oz	1.30
			Prepreg	7628HRC*2	17.06	15.76
6	Sig 3		Copper foil		1.0oz	1.30
			Core	3mil H/1	3.00	3.00
7	GND		Copper foil		0.5oz	0.70
			Prepreg	1080LRC	2.80	2.67
8	Bottom		Copper foil		0.5oz	0.70
			Add Plating		1.3	1.40
			SolderMask		0.6	0.50
Overall Thickness (1.45 mm ± 10%)					57.00	1.4478

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SATA	DESTINATION
SATA 0	HDD
SATA 1	ODD/ E3 Module Bay
SATA 2	NA
SATA 3	NA
SATA 4	ESATA
SATA 5	Dock

PCH	USB PORT#	DESTINATION
	0	JUSB1 (Ext Right Side)
	1	JESA1 (Ext Right Side)
	2	IO Board- JUSB1 (Ext Left Side)
	3	IO Board- JUSB2 (Ext Left Side)
	4	WLAN
	5	WWAN
	6	JMINI3(Pink Panther)
	7	USH->BIO
	8	DOCKING
	9	DOCKING
	10	Express card
	11	Bluetooth
	12	Camera
	13	LCD Touch
USH	0	BIO
	1	NA

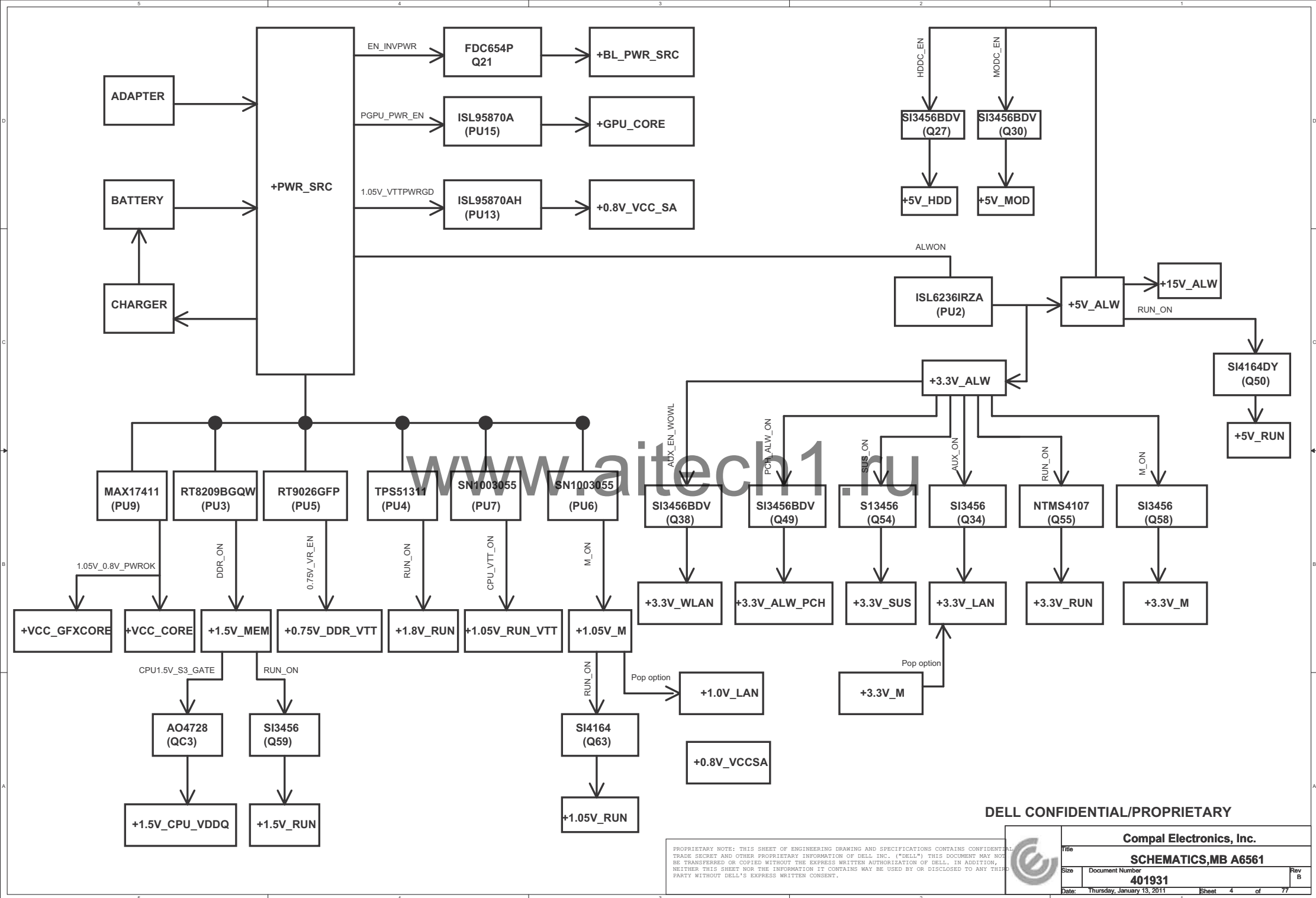
DSC DP/HDMI Port	Connetion
Port C	Dock DP port 2
Port D	Dock DP port 1
Port E	MB HDMI Conn

PCI EXPRESS	DESTINATION
Lane 1	MINI CARD-1 WWAN
Lane 2	MINI CARD-2 WLAN
Lane 3	Express card
Lane 4	E3 Module Bay (USB3)
Lane 5	MINI CARD-3 (Pink Panther)
Lane 6	MMI
Lane 7	10/100/1G LOM
Lane 8	None

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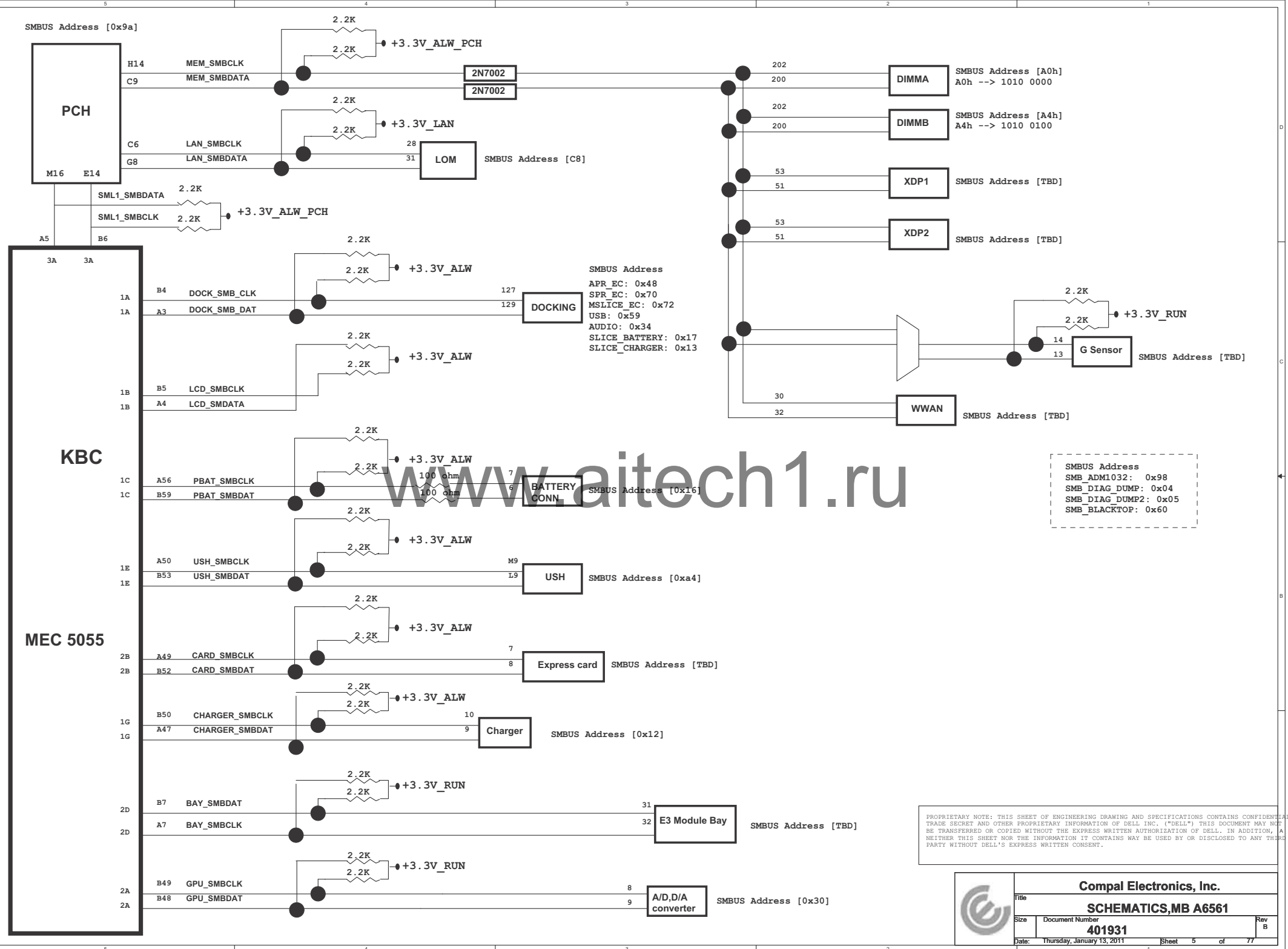
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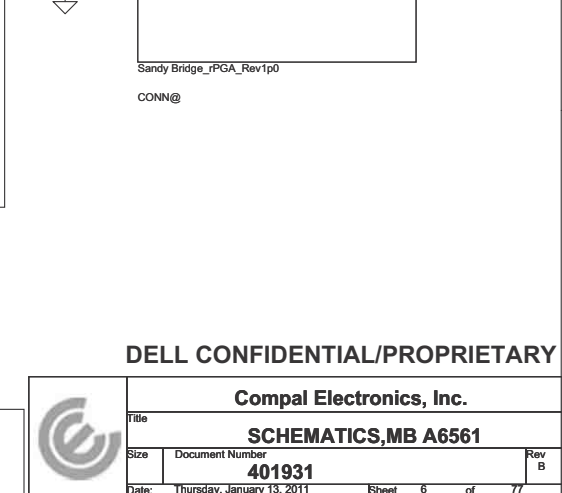
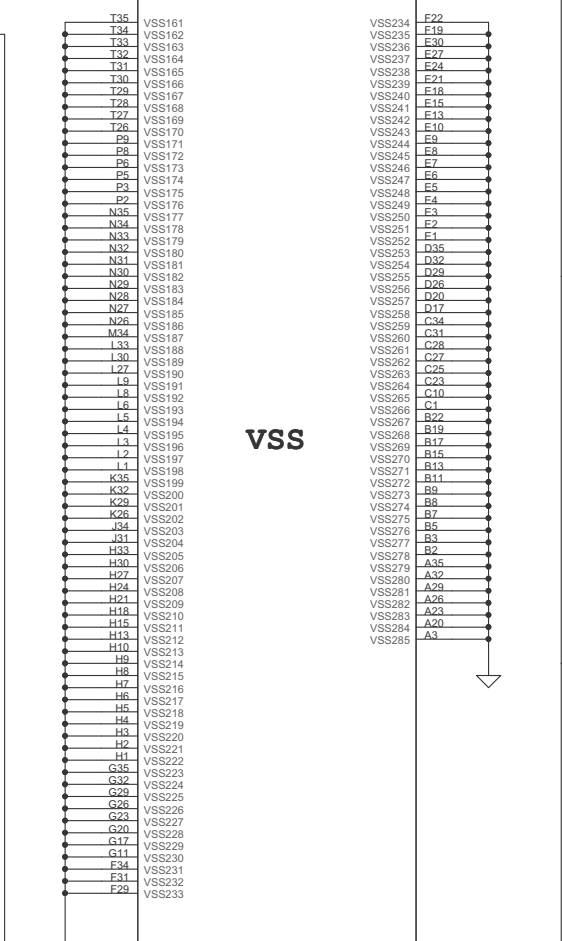


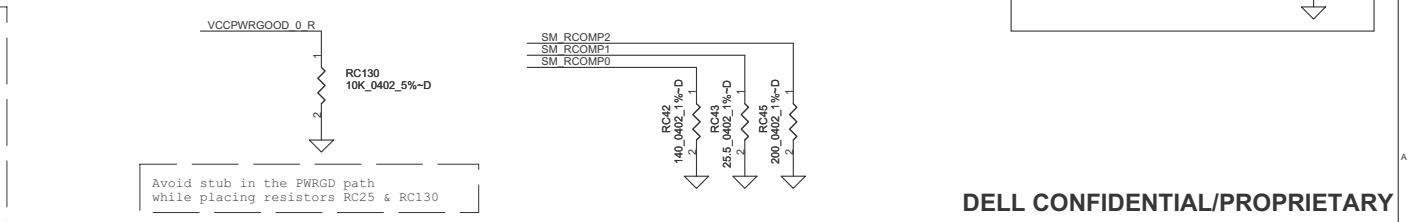
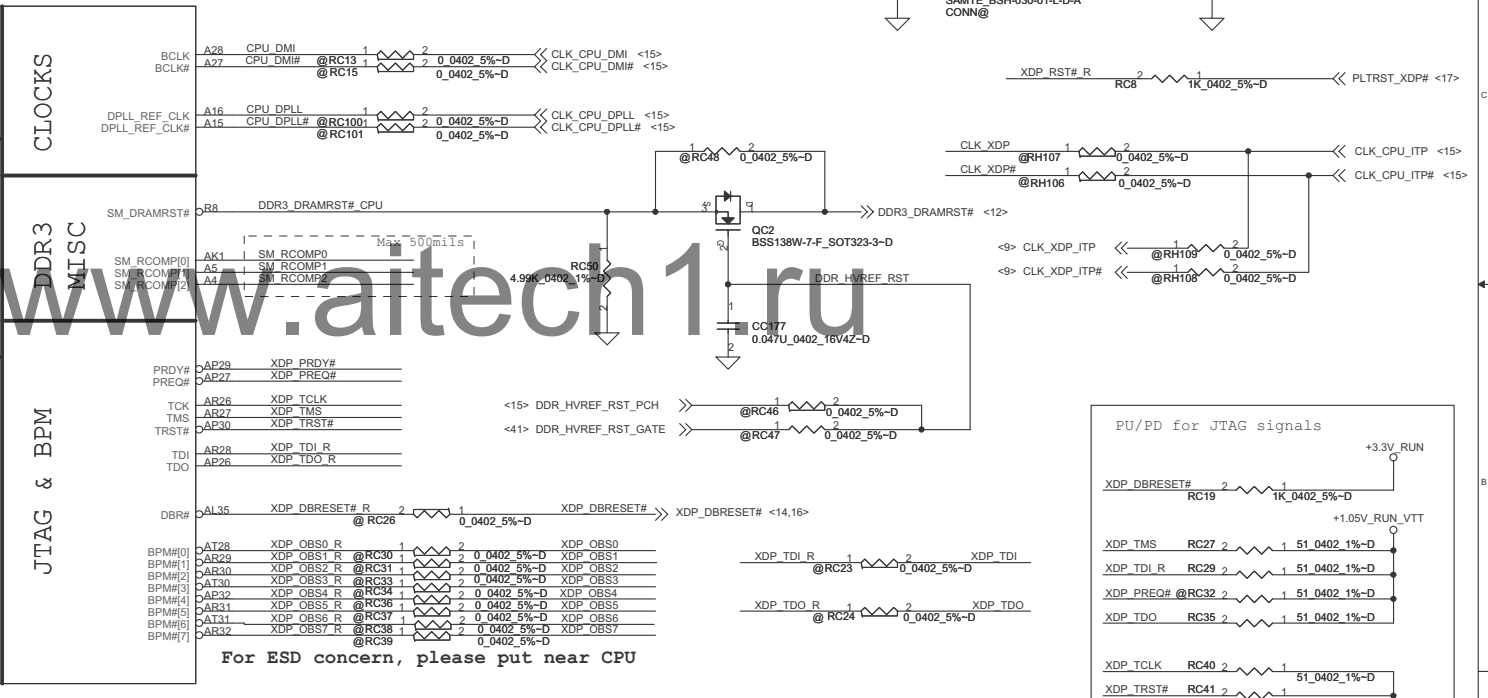
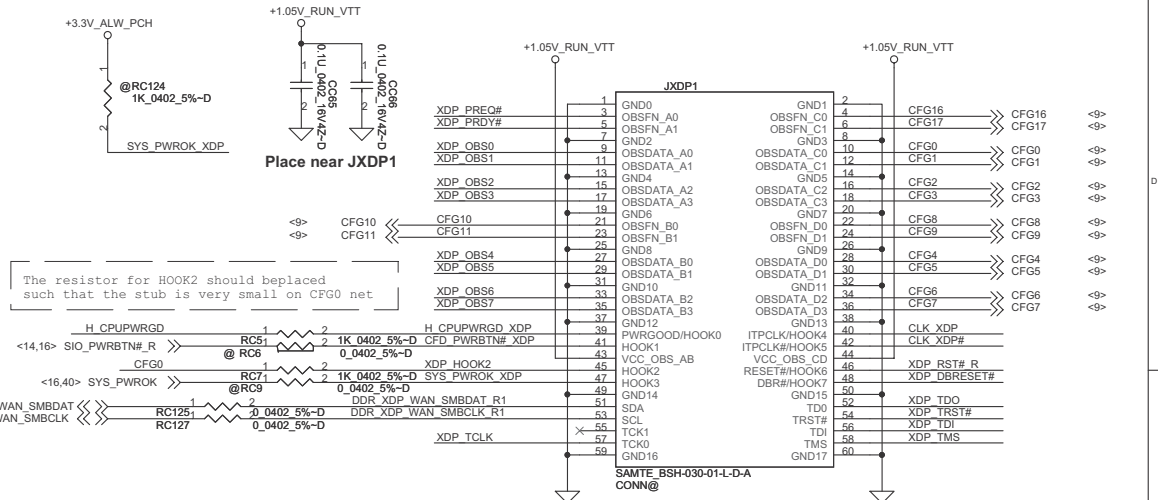
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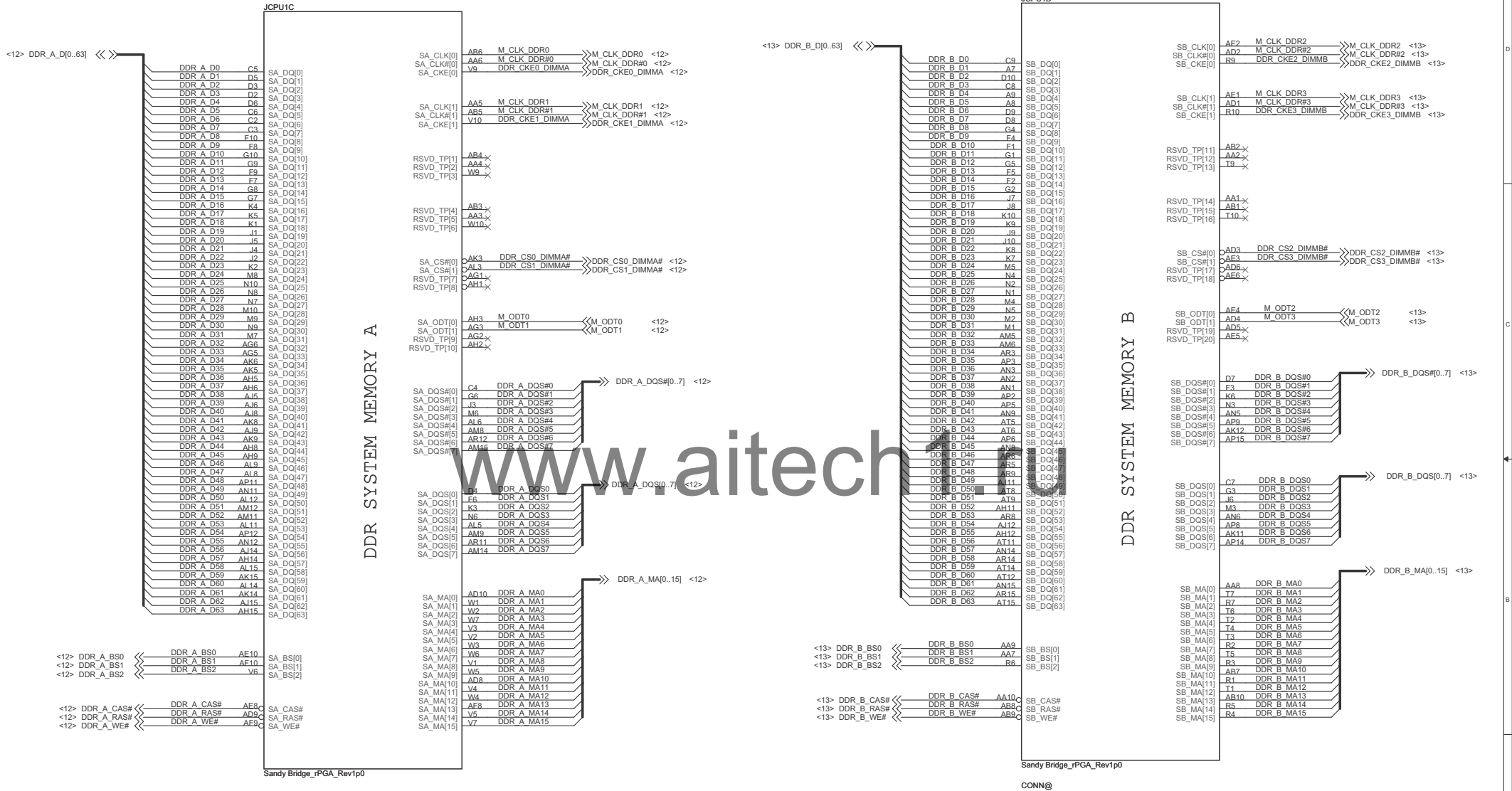






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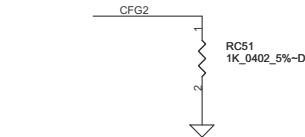
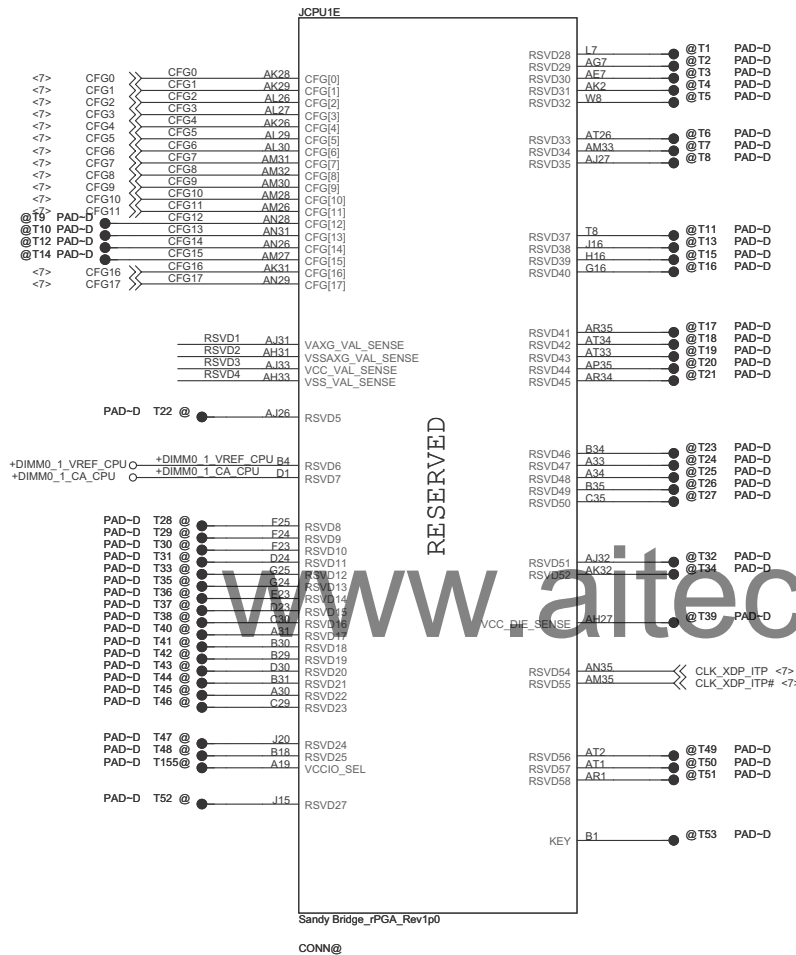
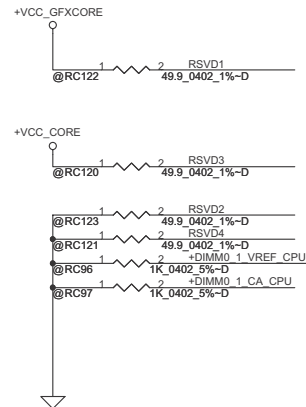
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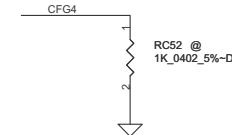
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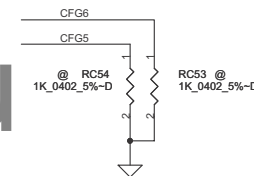
CFG Straps for Processor



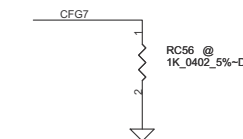
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: (Default) Normal Operation; Lane # definition matches socket pin map definition 0: Lane Reversed



Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIe Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xRESETB de assertion 0: PEG Wait for BIOS for training

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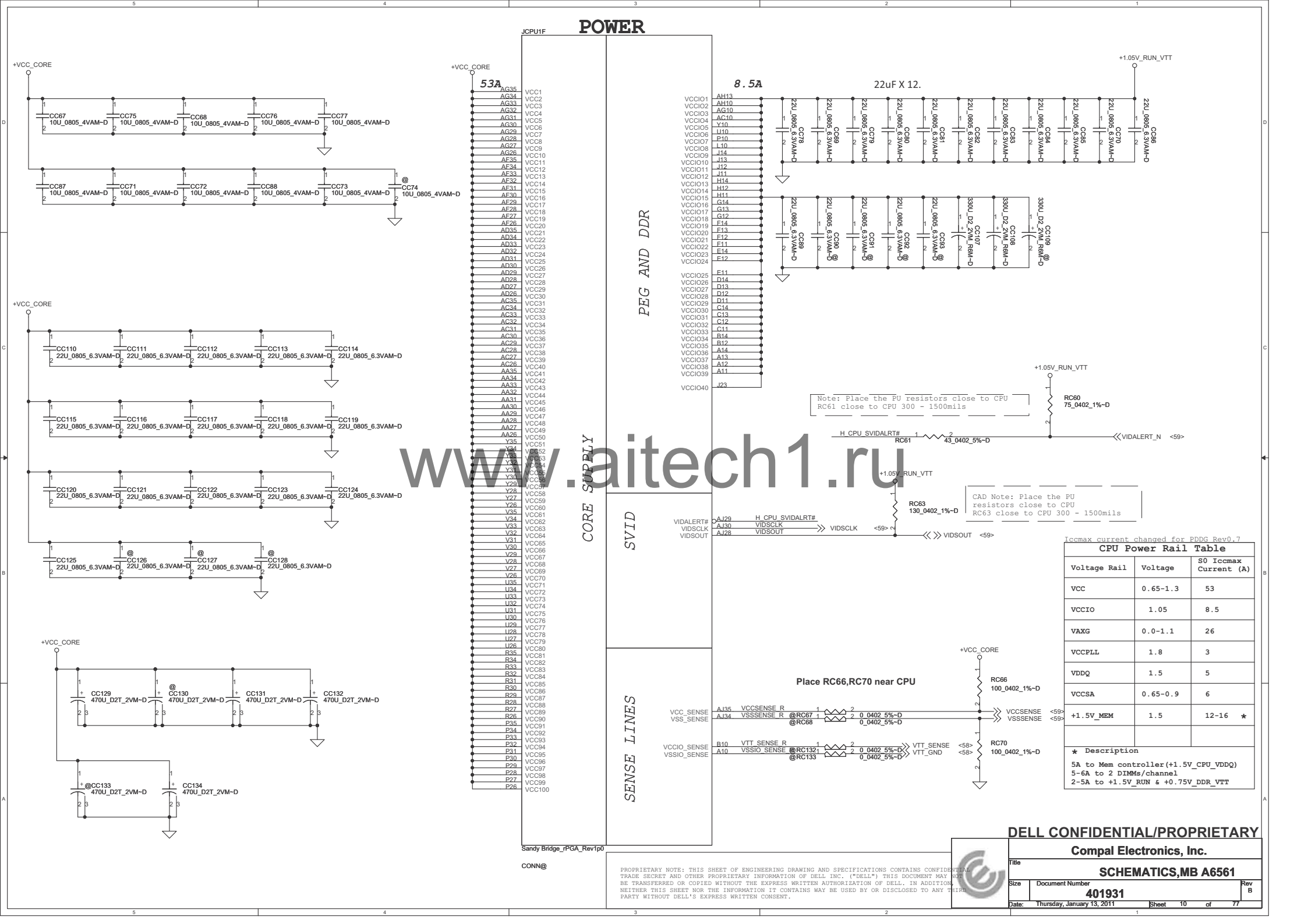
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POWER

PEG AND DDR

CORE SUPPLY

SVID

SENSE LINES

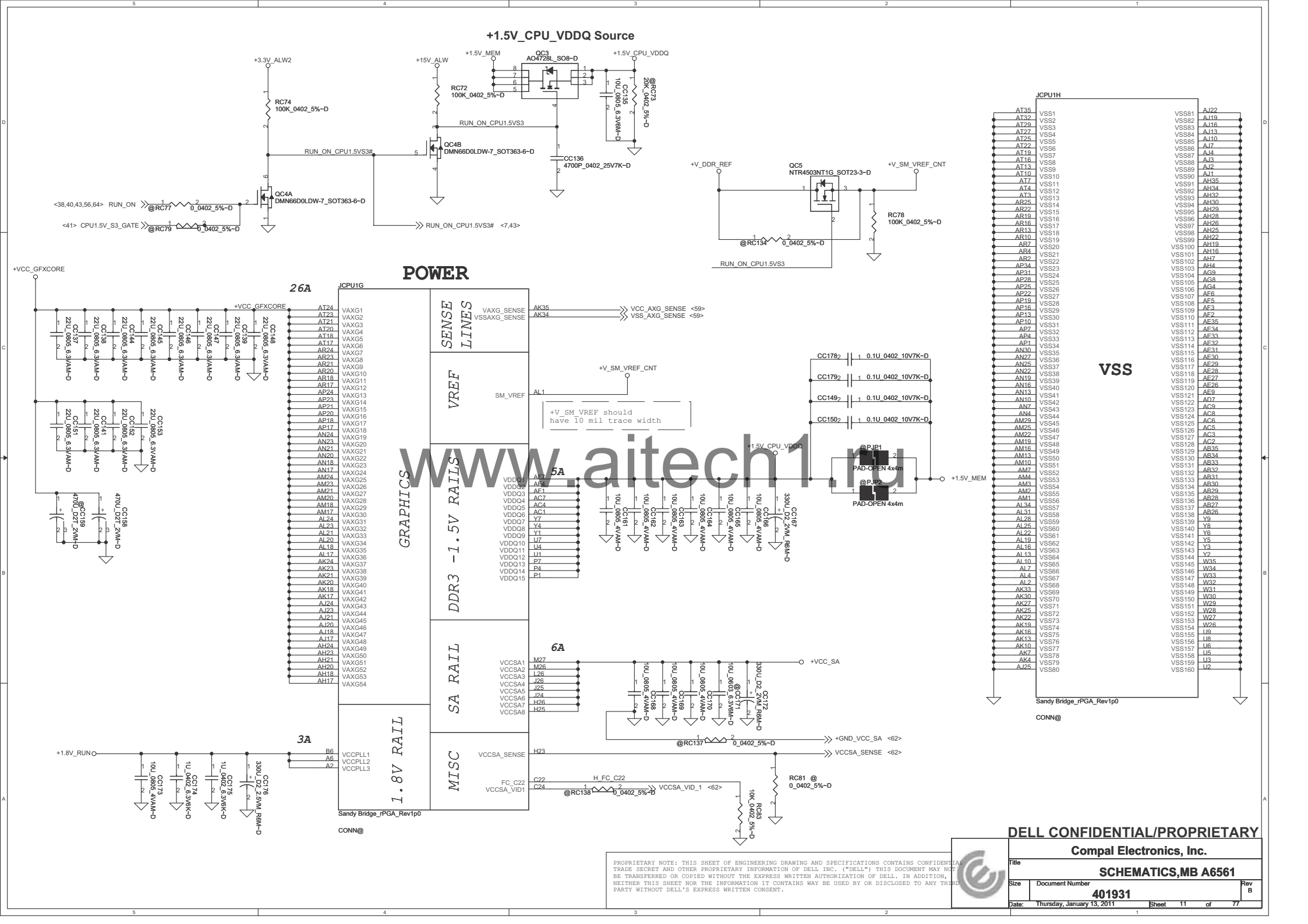
Iccmax current changed for PDDG Rev0.7		
CPU Power Rail Table		
Voltage Rail	Voltage	S0 Iccmax Current (A)
VCC	0.65-1.3	53
VCCIO	1.05	8.5
VAXG	0.0-1.1	26
VCCPLL	1.8	3
VDDQ	1.5	5
VCCSA	0.65-0.9	6
+1.5V_MEM	1.5	12-16 *
* Description		
5A to Mem controller(+1.5V_CPU_VDDQ)		
5-6A to 2 DIMMs/channel		
2-5A to +1.5V_RUN + +0.75V_DDR_VTT		

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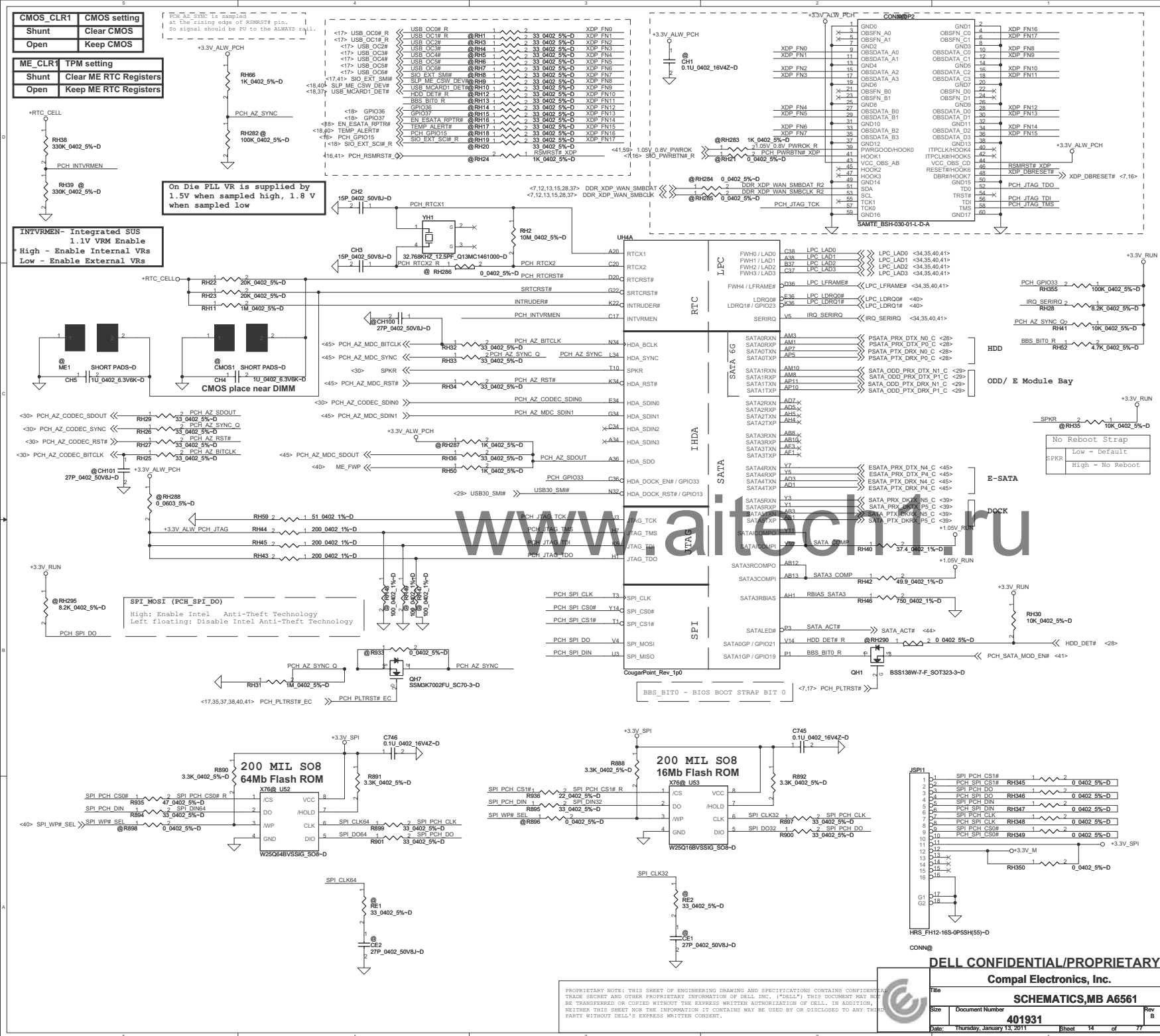
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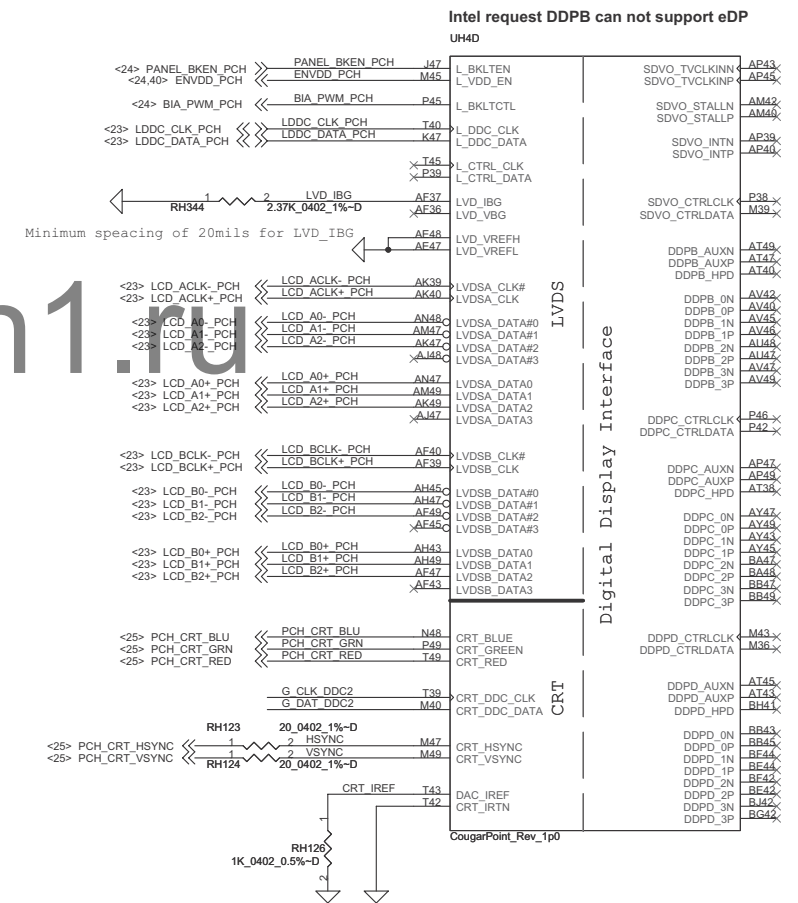
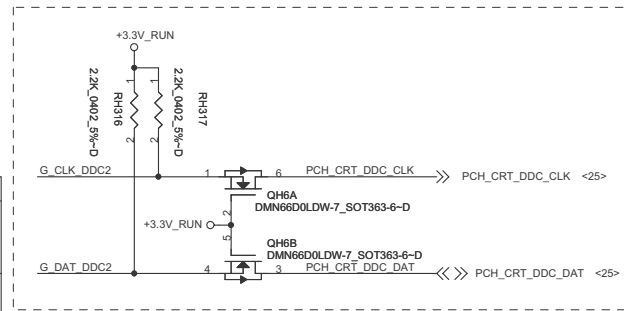


UH4B

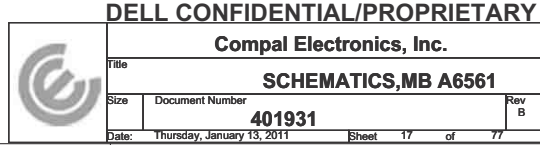
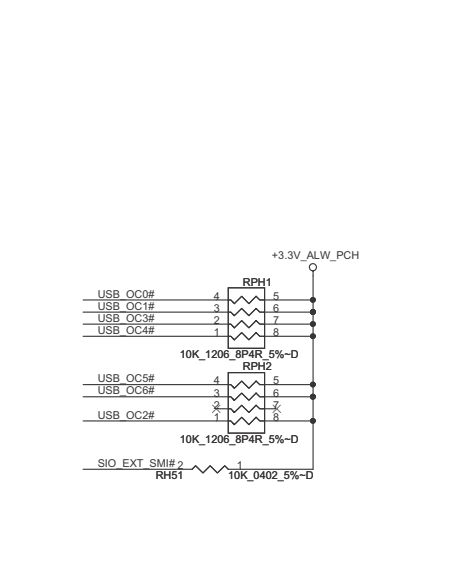
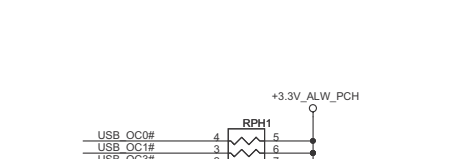
CougarPoint Rev 1p0

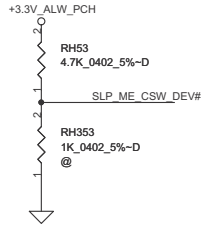
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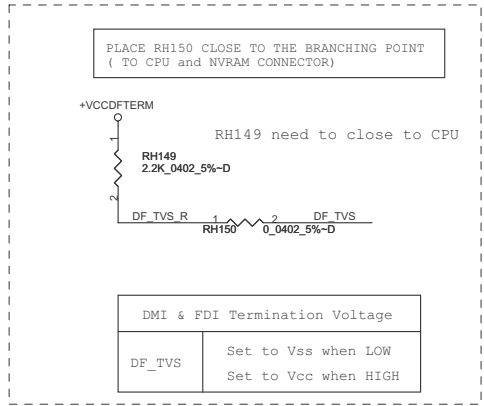
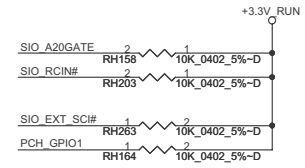
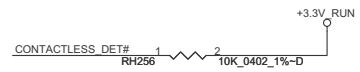
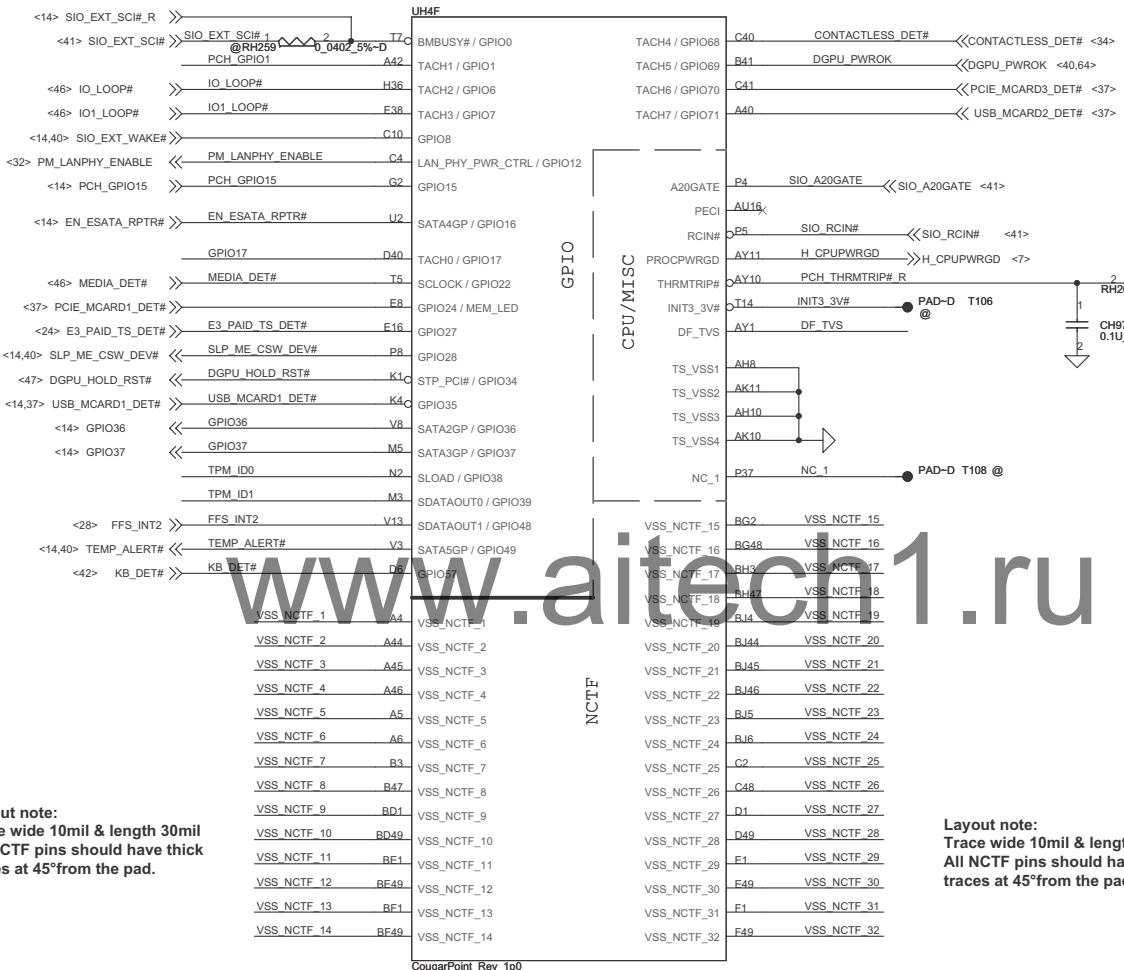
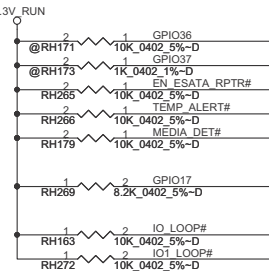
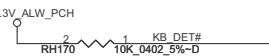
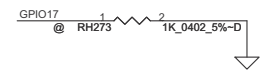
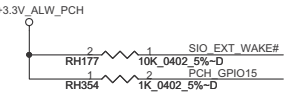
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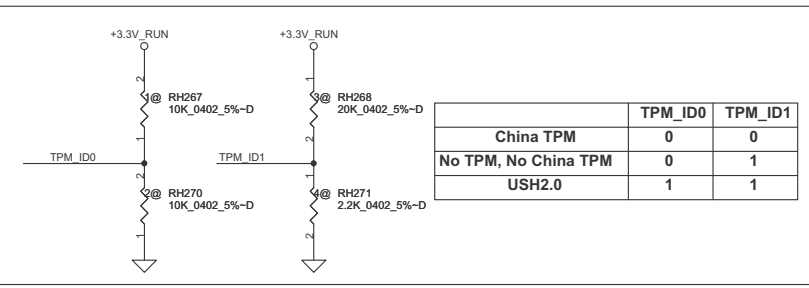
Note: PCH has internal pull up 20k ohm on E3_PAID_TS_DET# (GPIO27)

SLP_ME_CSW_DEV#	PLL ON DIE VR ENABLE
ENABLED - HIGH DEFAULT	
DISABLED - LOW	



Layout note:
Trace wide 10mil & length 30mil
All NCTF pins should have thick traces at 45° from the pad.

Layout note:
Trace wide 10mil & length 30mil
All NCTF pins should have thick traces at 45° from the pad.



	TPM_ID0	TPM_ID1
China TPM	0	0
No TPM, No China TPM	0	1
USH2.0	1	1

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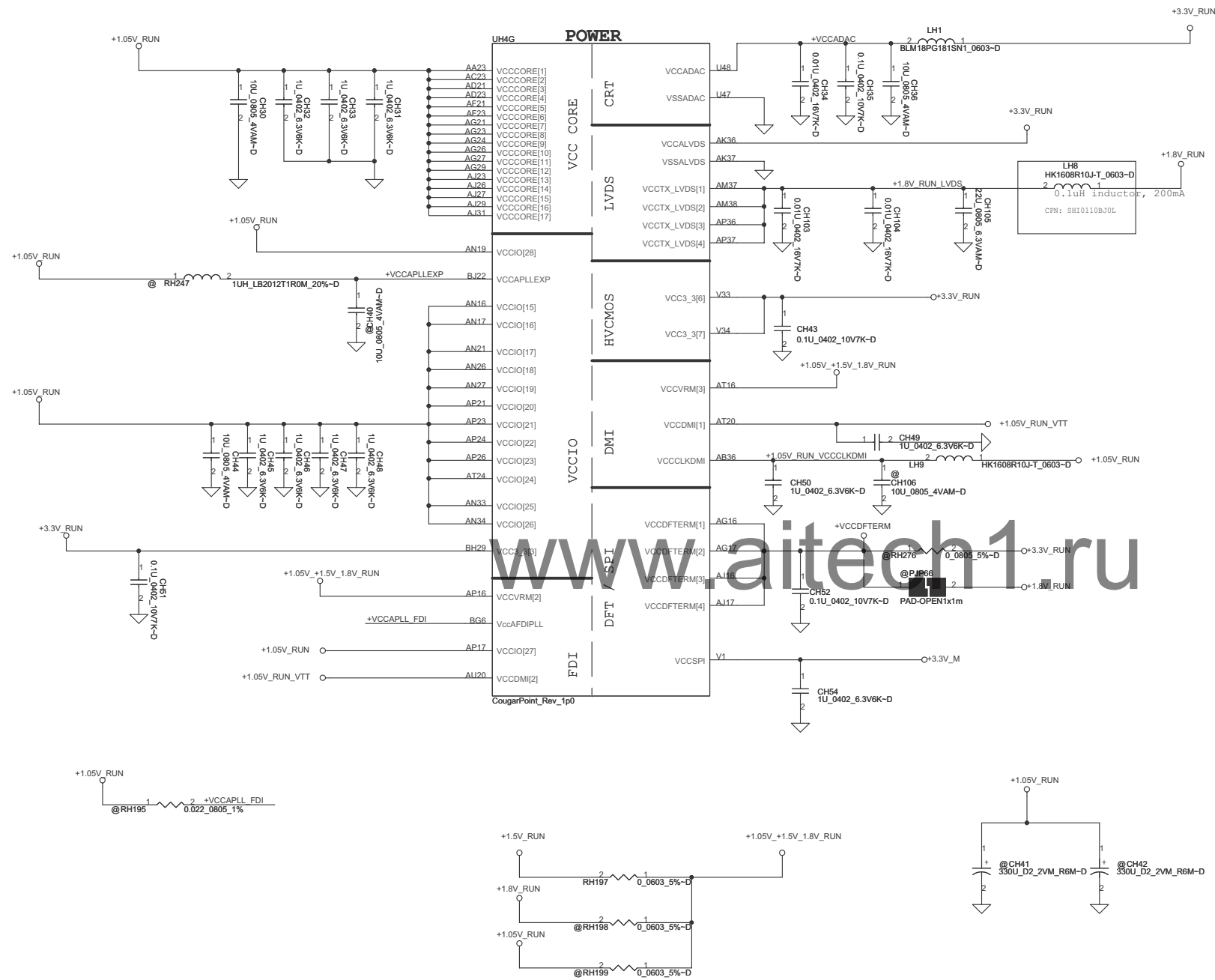
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PCH Power Rail Table		
Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC3	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.020
VccDSW3_3	3.3	0.003
VccpDFTerm	1.8	0.19
VccRTC	3.3	2 (mA)
VccSus3_3	3.3	0.119
VccSusHDA	3.3	0.01
VccVRM	1.8 / 1.5	0.16
VccClkDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.06
VccAPLLEXP	1.05	0.05

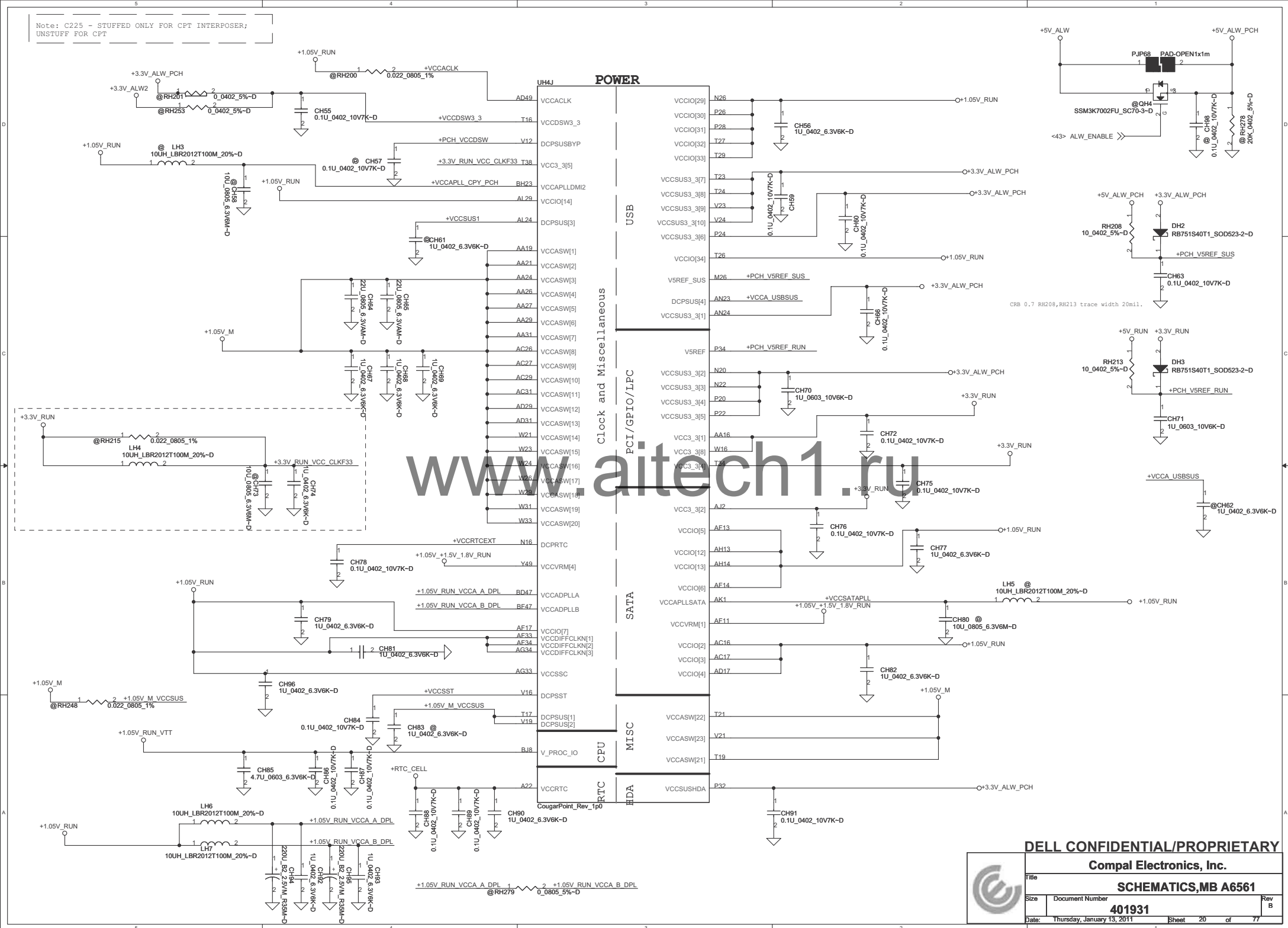
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Note: C225 - STUFFED ONLY FOR CPT INTERPOSER;
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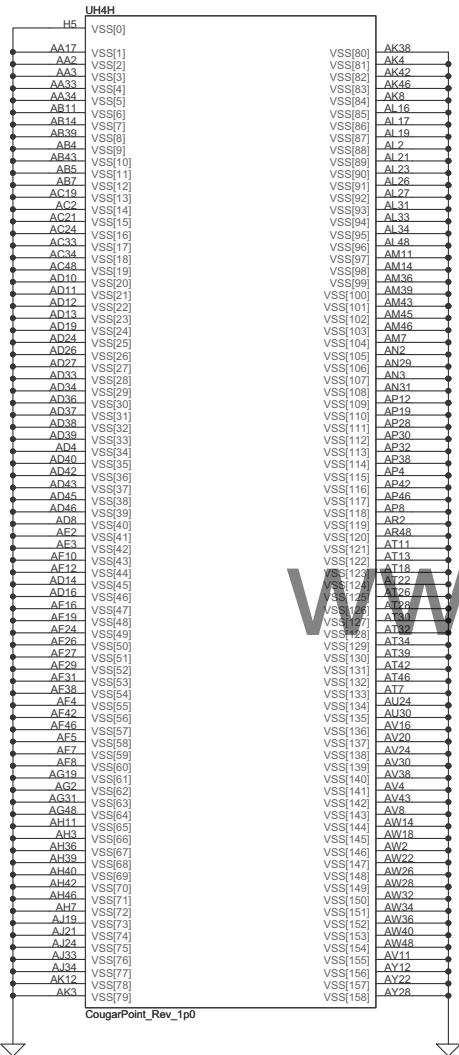
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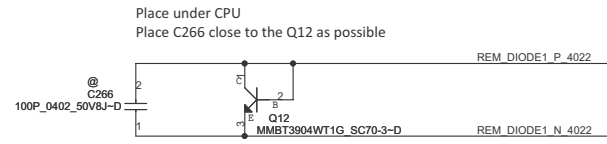


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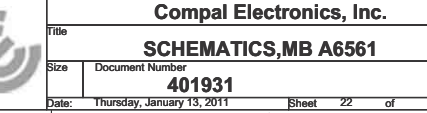
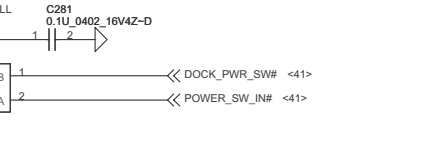
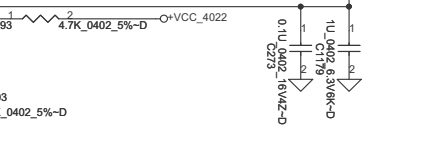
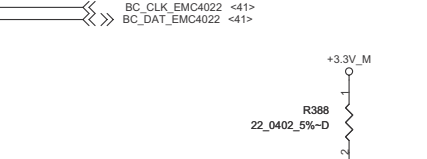
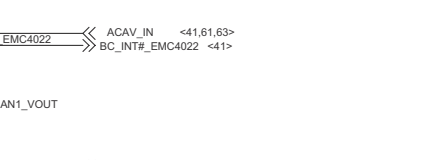
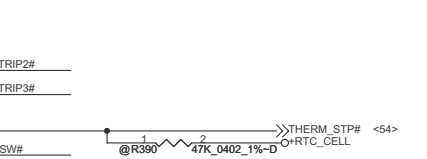
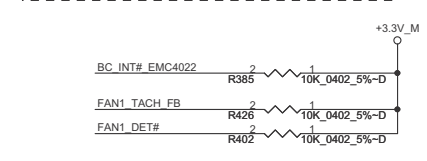
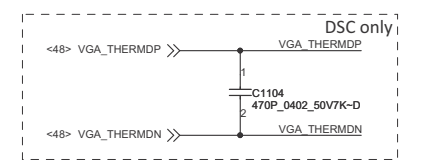
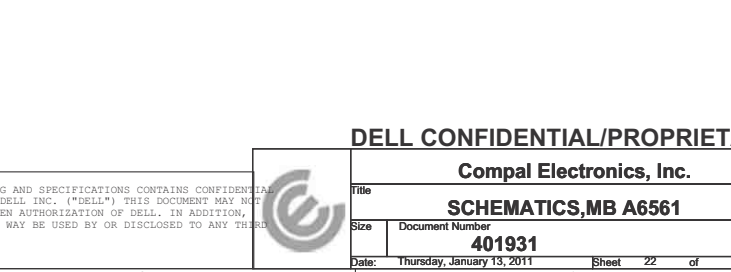
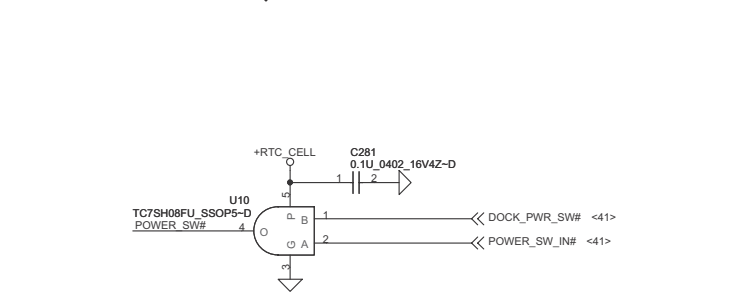
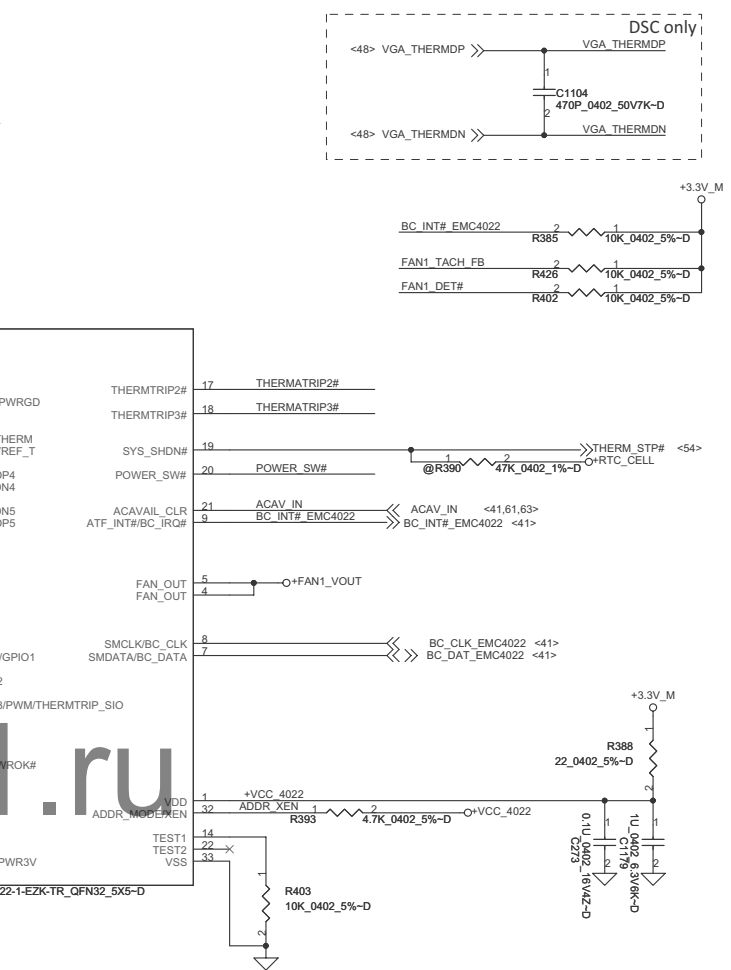
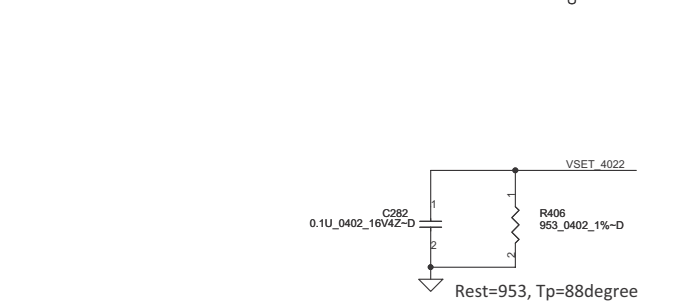
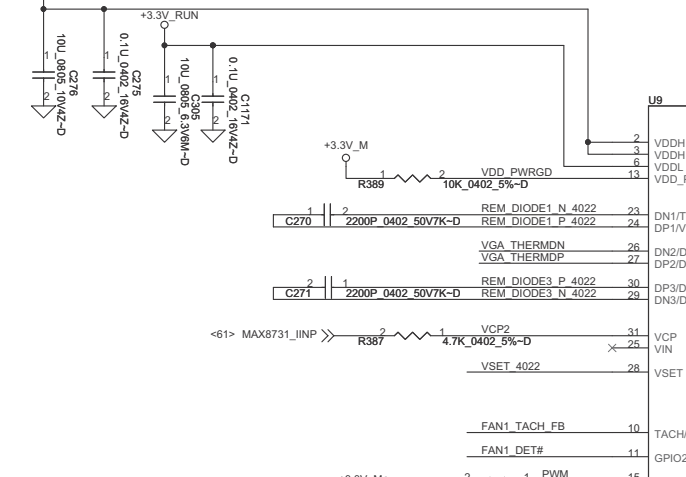
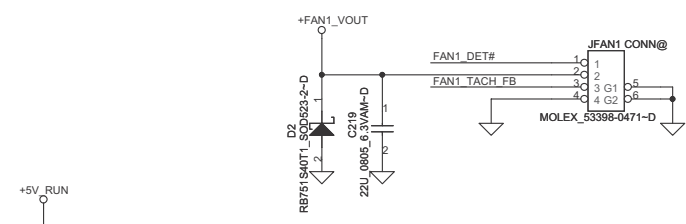
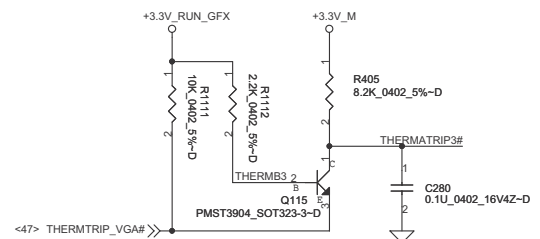
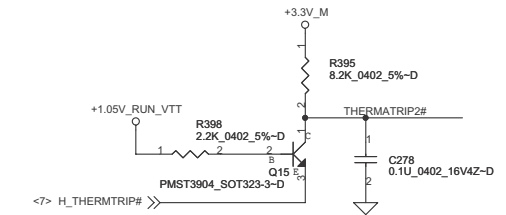
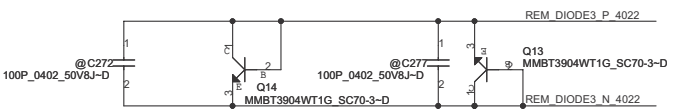
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DP3/DN3 for SODIMM on Q14, place Q14 close to SODIMM and C272 close to Q14
DP5/DN5 for Skin on Q13, place Q13 close to JMINI1 for WWAN and C277 close Q13.

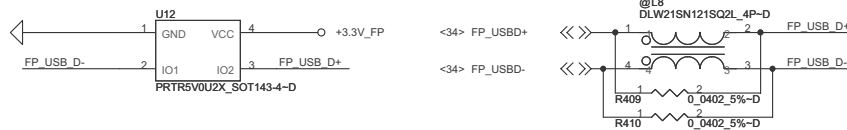
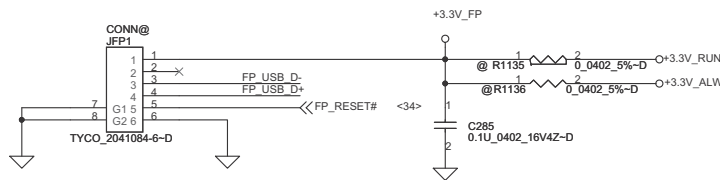
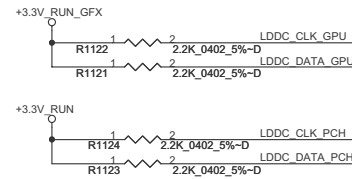
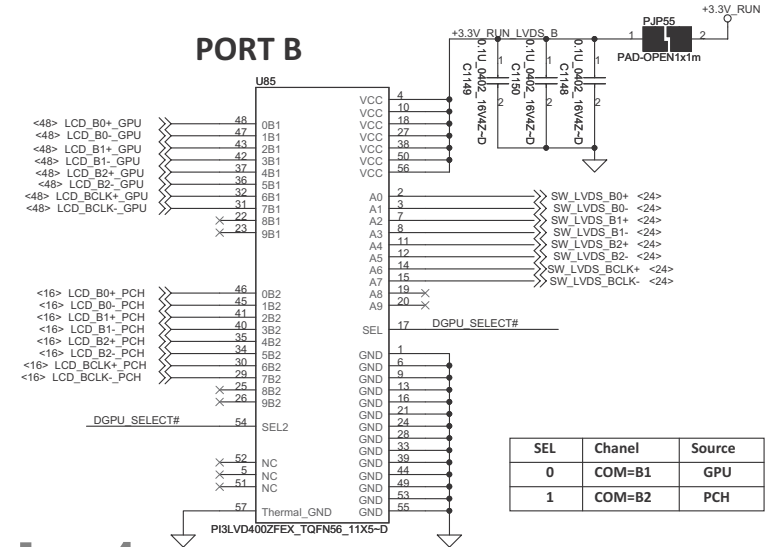
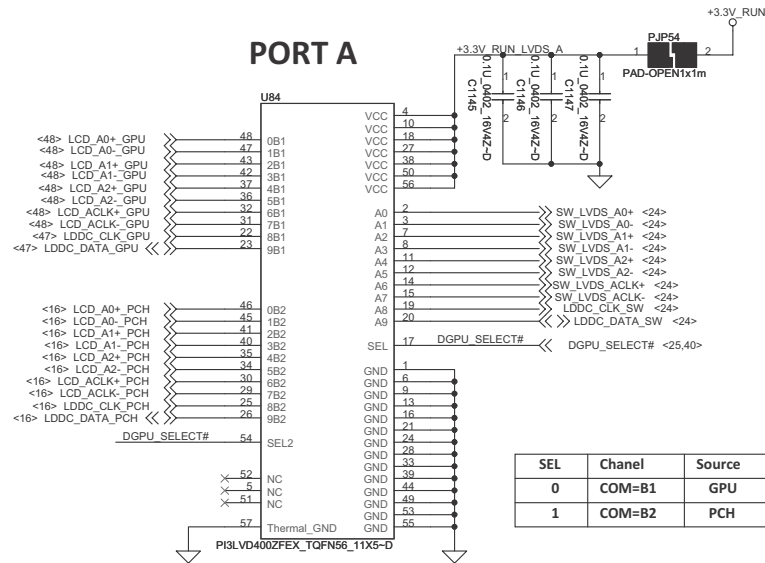


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LVDS SW

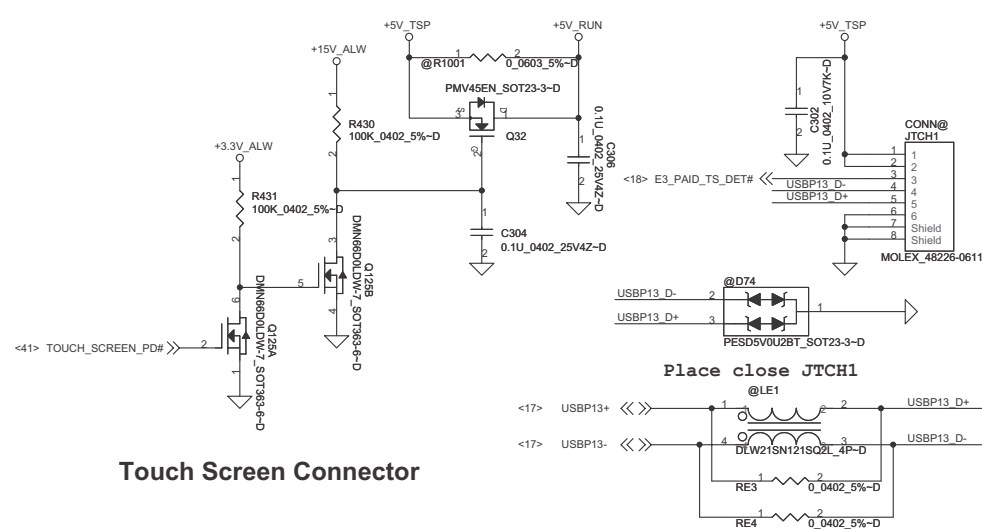
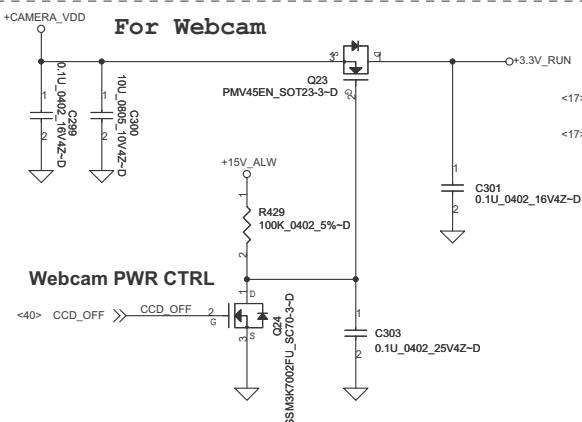
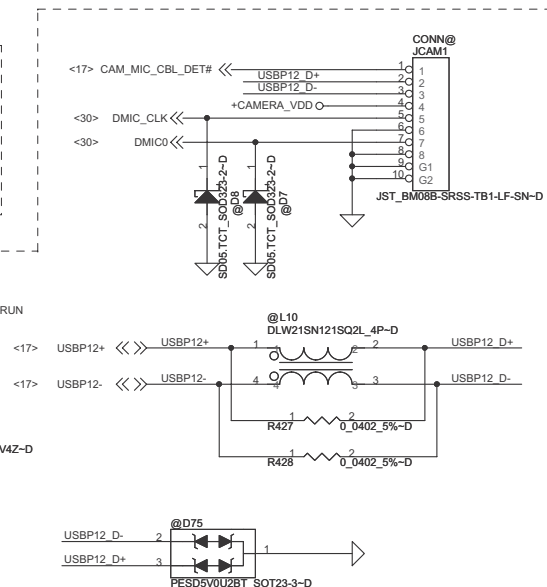
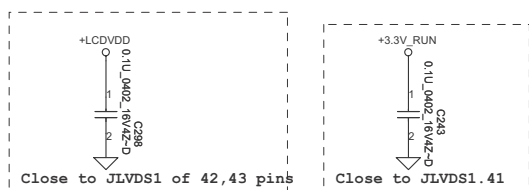
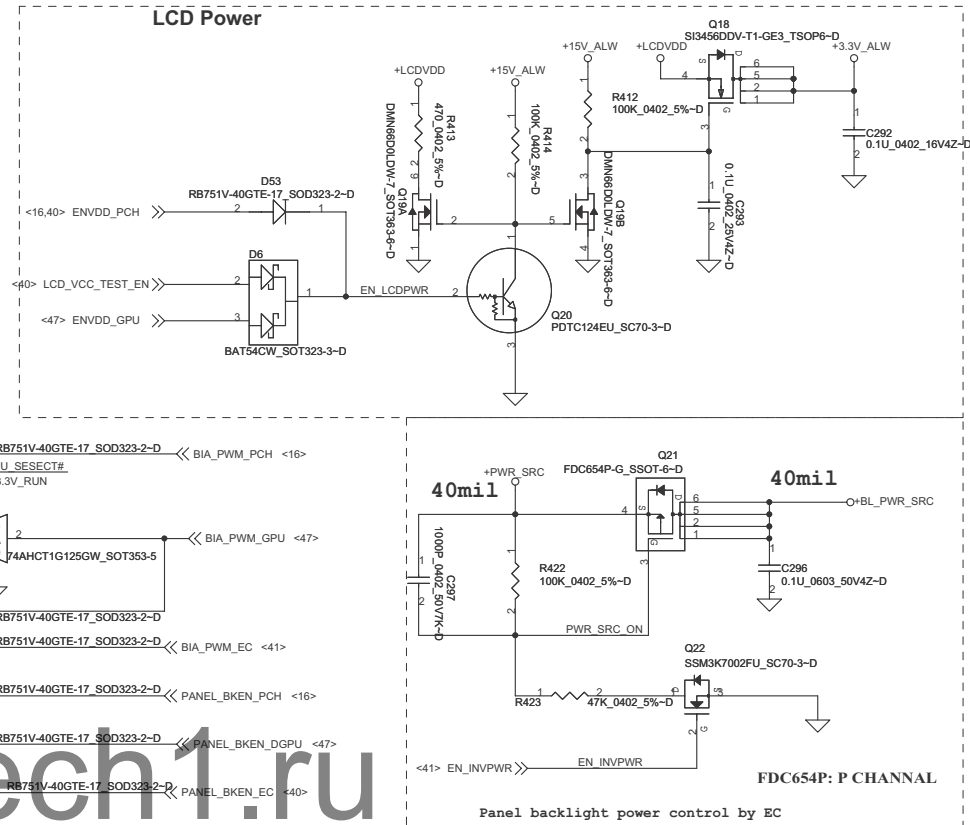
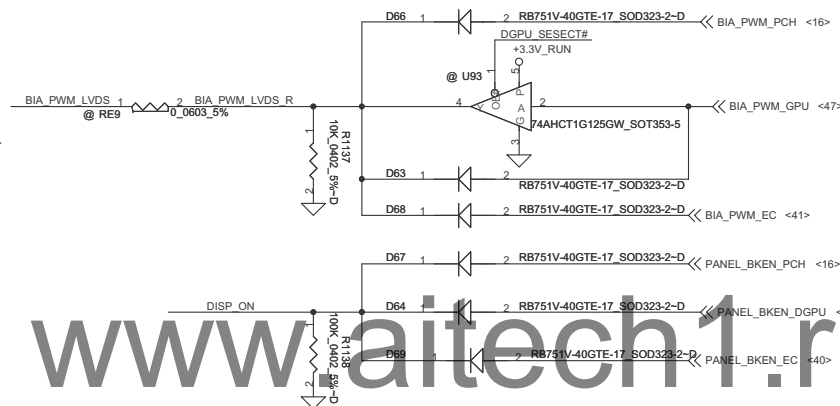
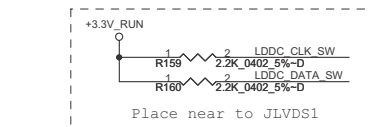


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Fingerprint CONN.

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Touch Screen Connector

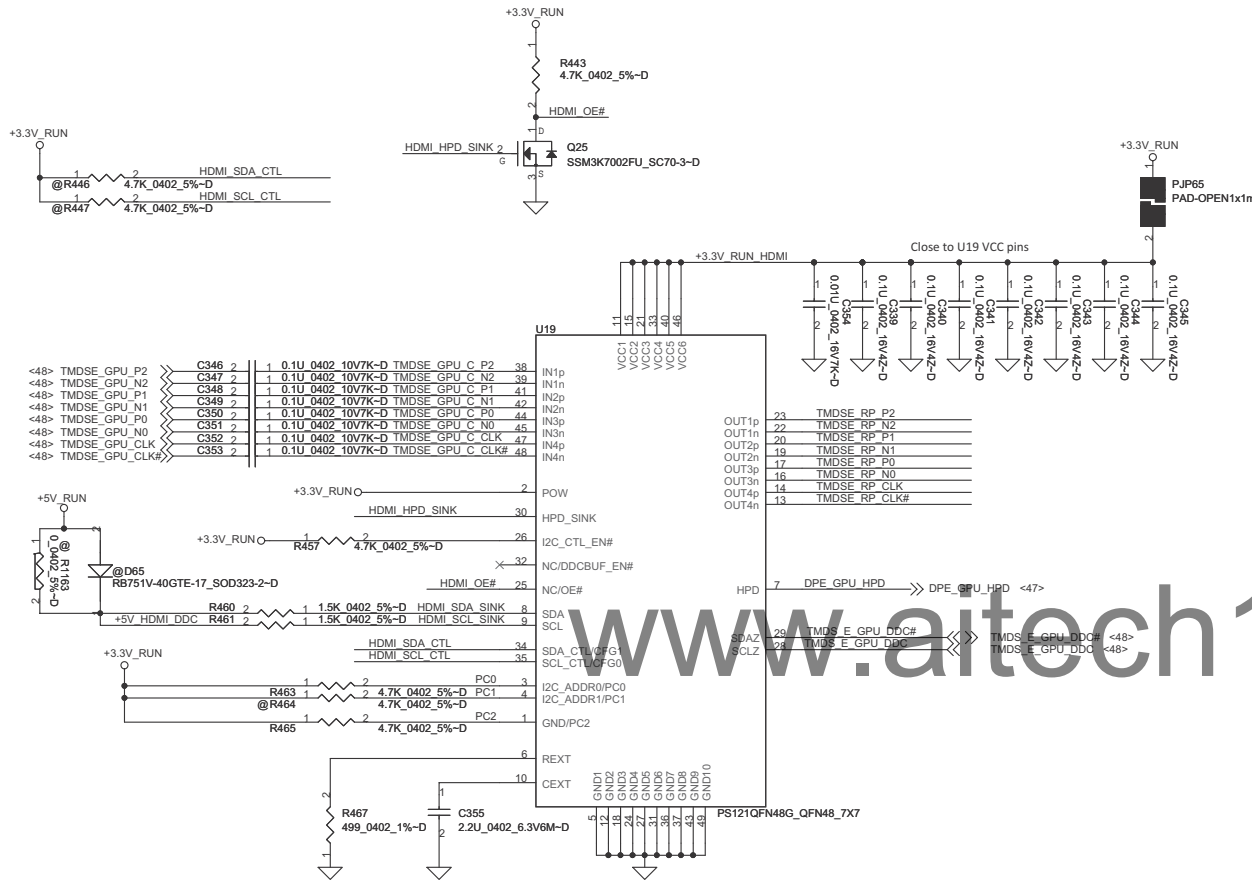
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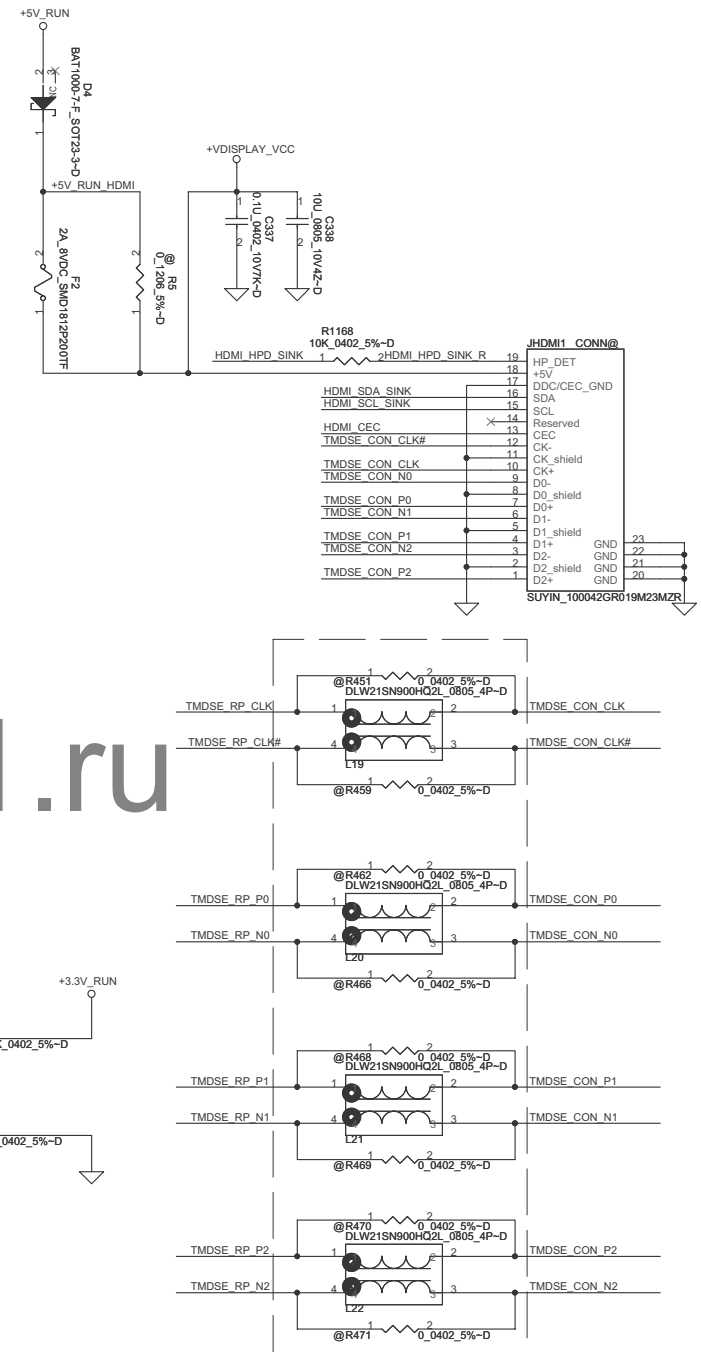
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EQUALIZATION SETTING:
 [PC2,PC1,PC0]=000, 12dB
 [PC2,PC1,PC0]=001, 16dB
 [PC2,PC1,PC0]=010, 10dB
 [PC2,PC1,PC0]=011, 7dB
 [PC2,PC1,PC0]=100, 1.5dB
 [PC2,PC1,PC0]=101, 4dB (Default)
 [PC2,PC1,PC0]=110, 9dB
 [PC2,PC1,PC0]=111, 7dB



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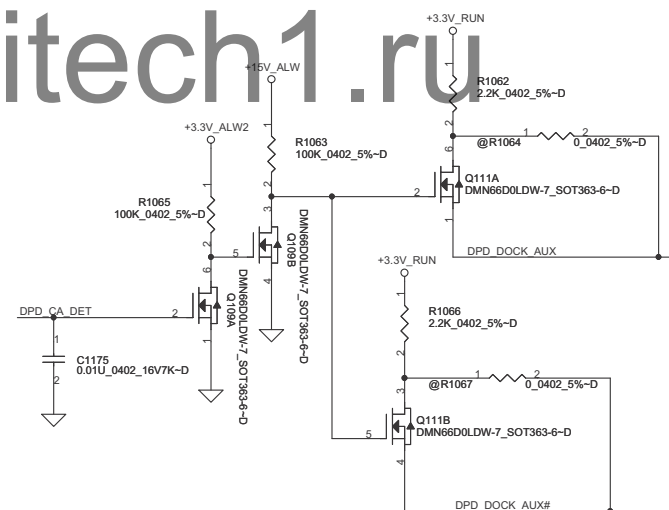
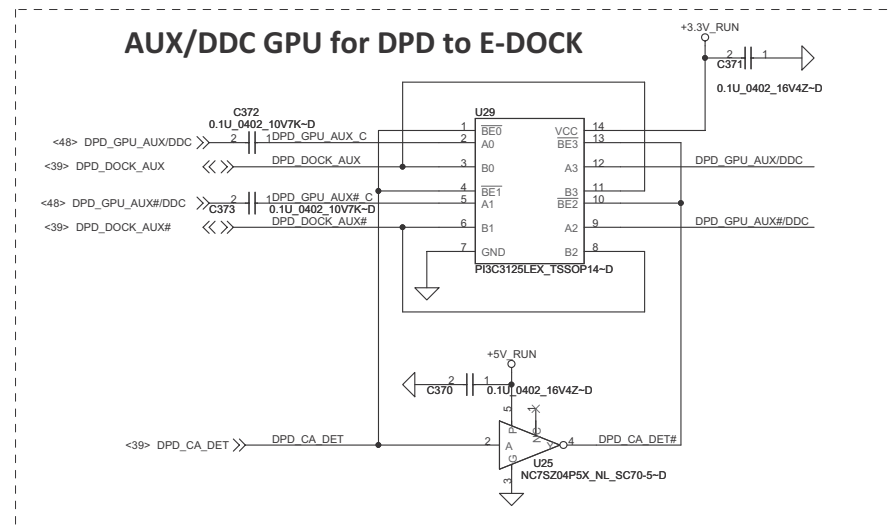
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AUX/DDC GPU for DPD to E-DOCK



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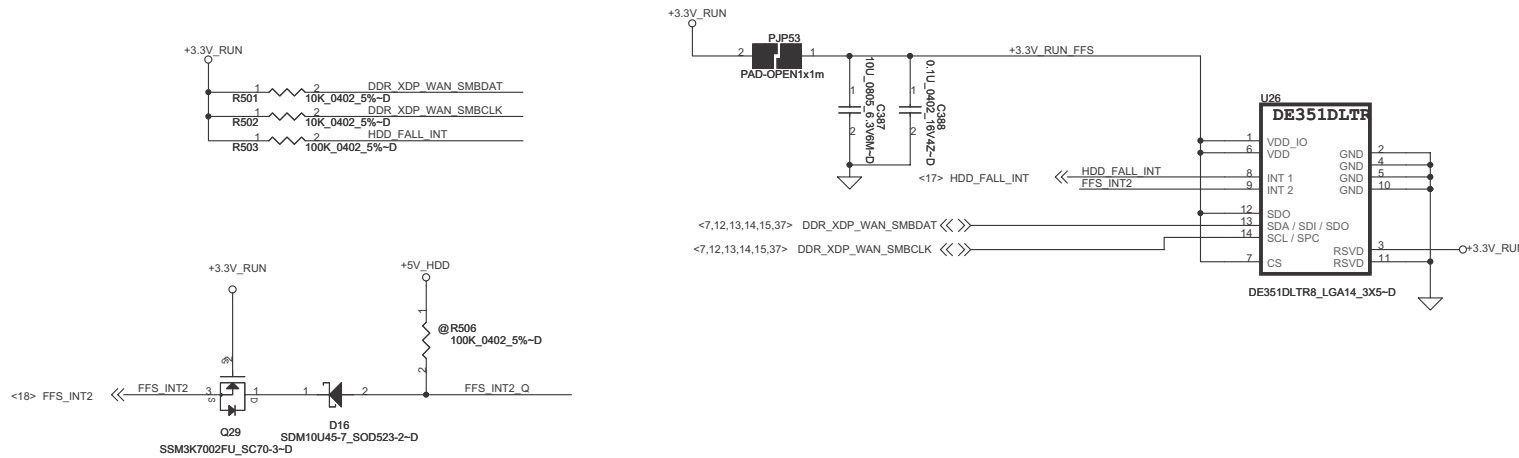
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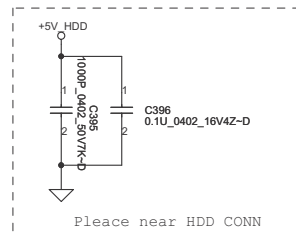
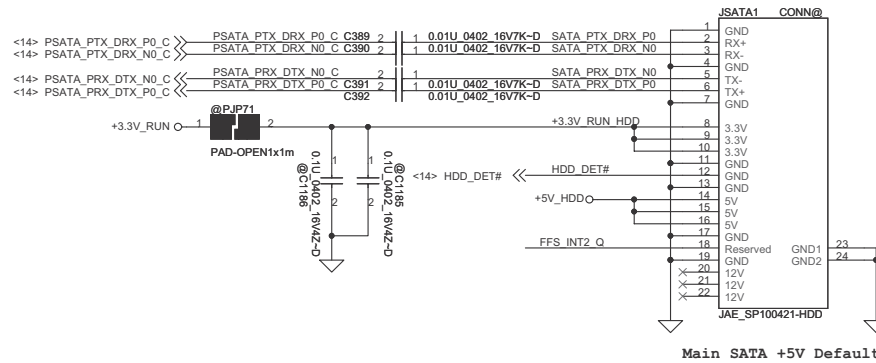
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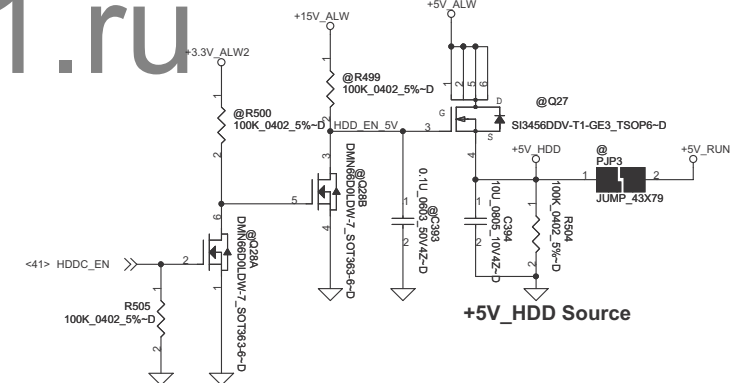
Free Fall Sensor



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For HDD Temp.



HDD PWR



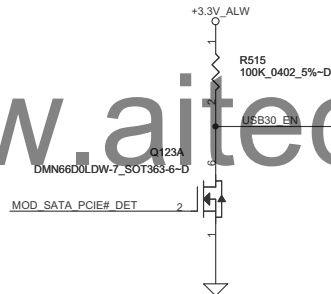
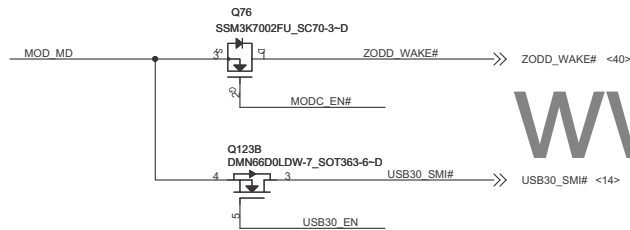
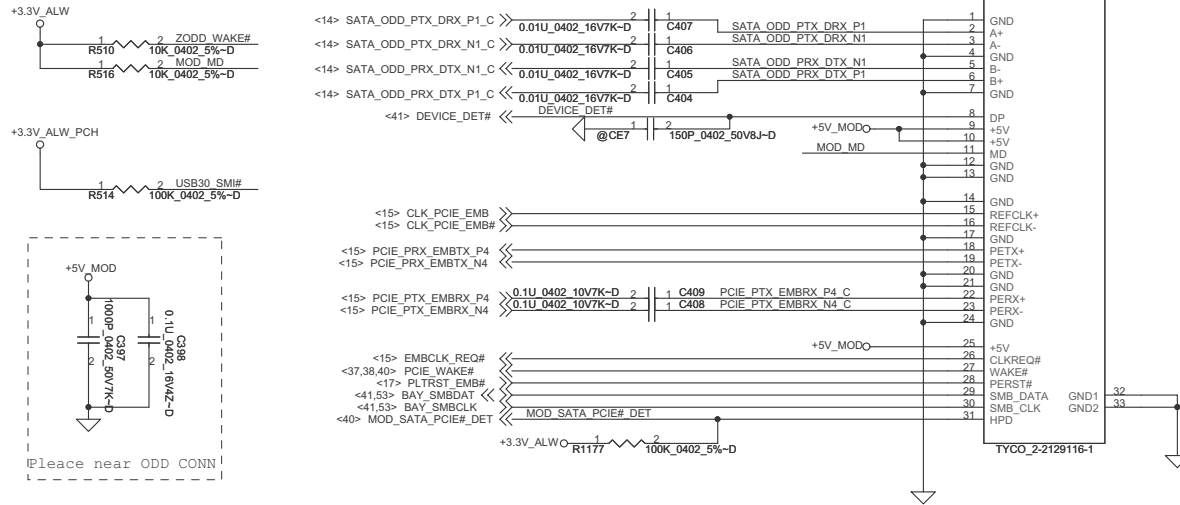
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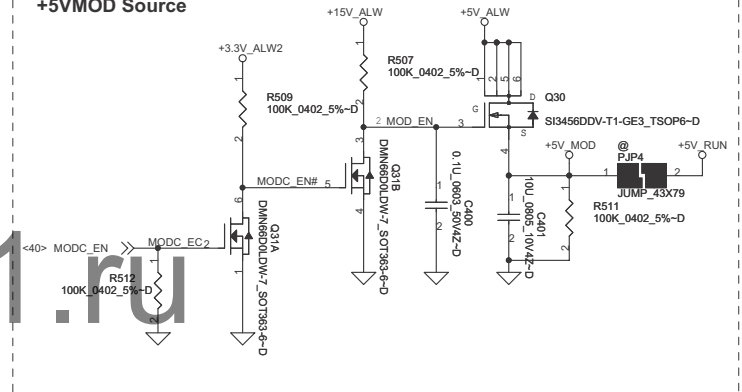
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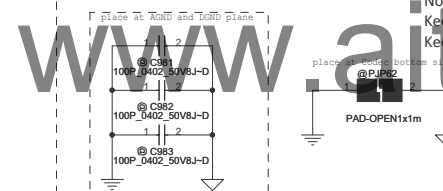
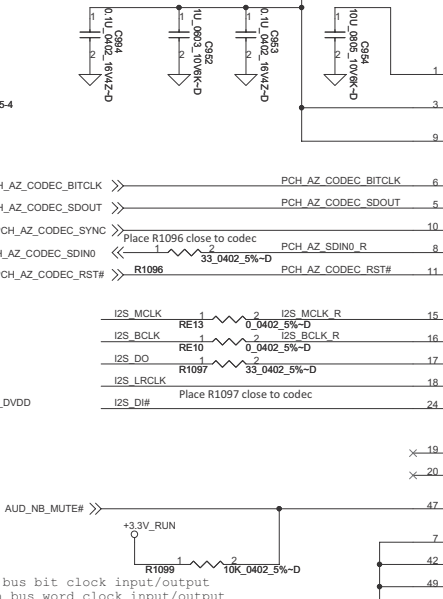
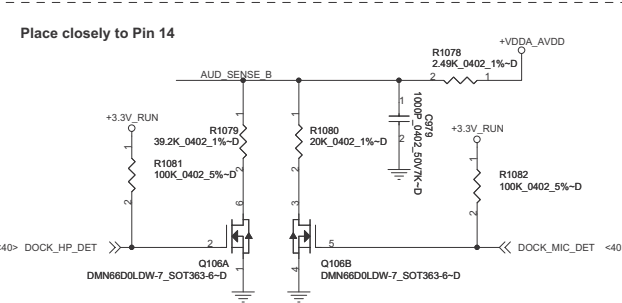
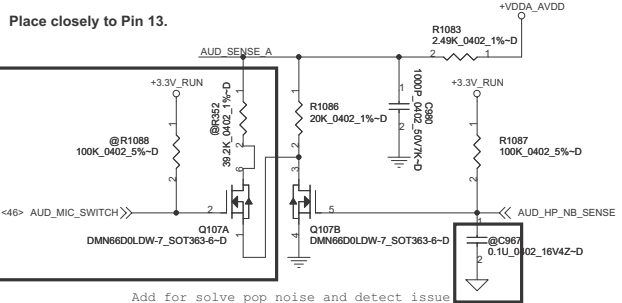
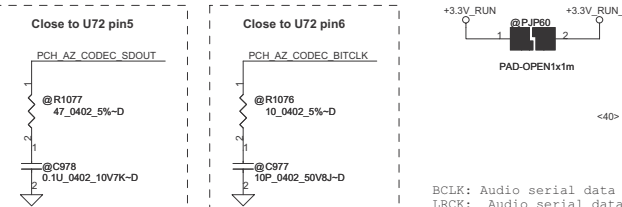
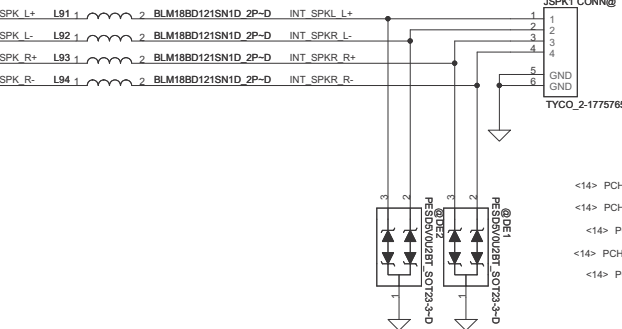
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Internal Speakers Header

DVDD_IO should match with HDA Bus level

15 mils trace

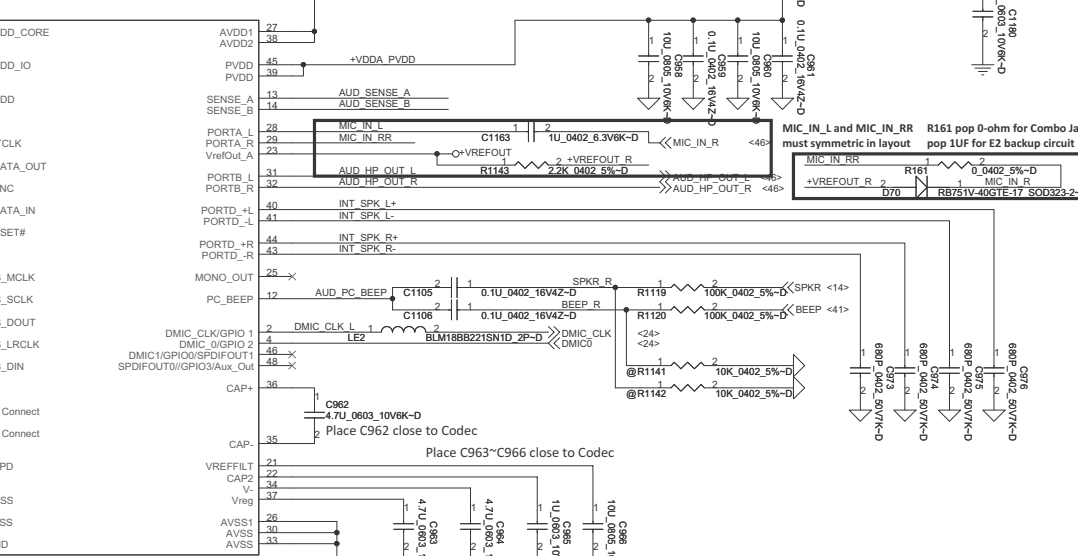
15 mils trace



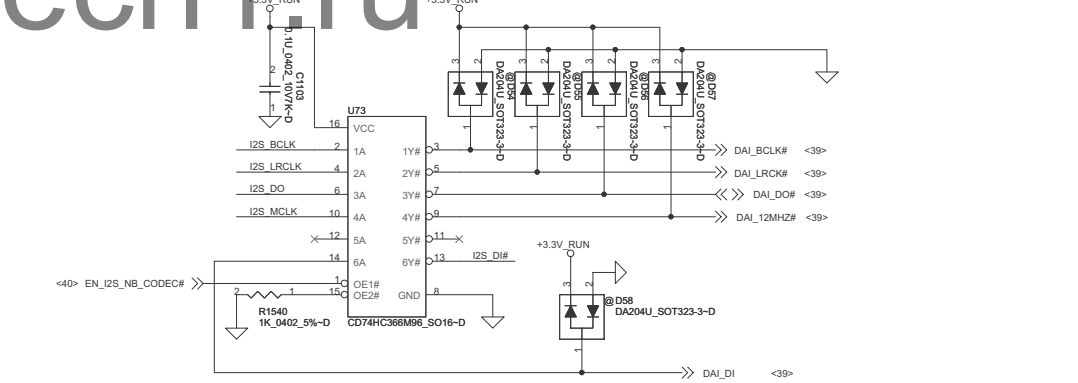
Resistor	SENSE_A	SENSE_B
39.2K	PORT A	PORT E
20K	PORT B	PORT F
10K	NA	DMICO
5.11K	SPDIFOUT0	SPDIFOUT1 (DMIC1)
2.49K	Pull-up to AVDD	

PORT A	External MIC
PORT B	HeadPhone Out
PORT C	Dock Audio
PORT D	Internal SPK

Place C994, C952~C957 close to Codec



Notes:
Keep PVDD supply and speaker traces routed on the DGND plane.
Keep away from AGND and other analog signals



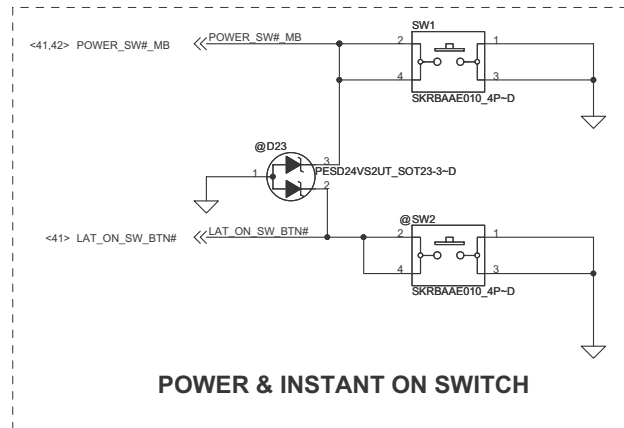
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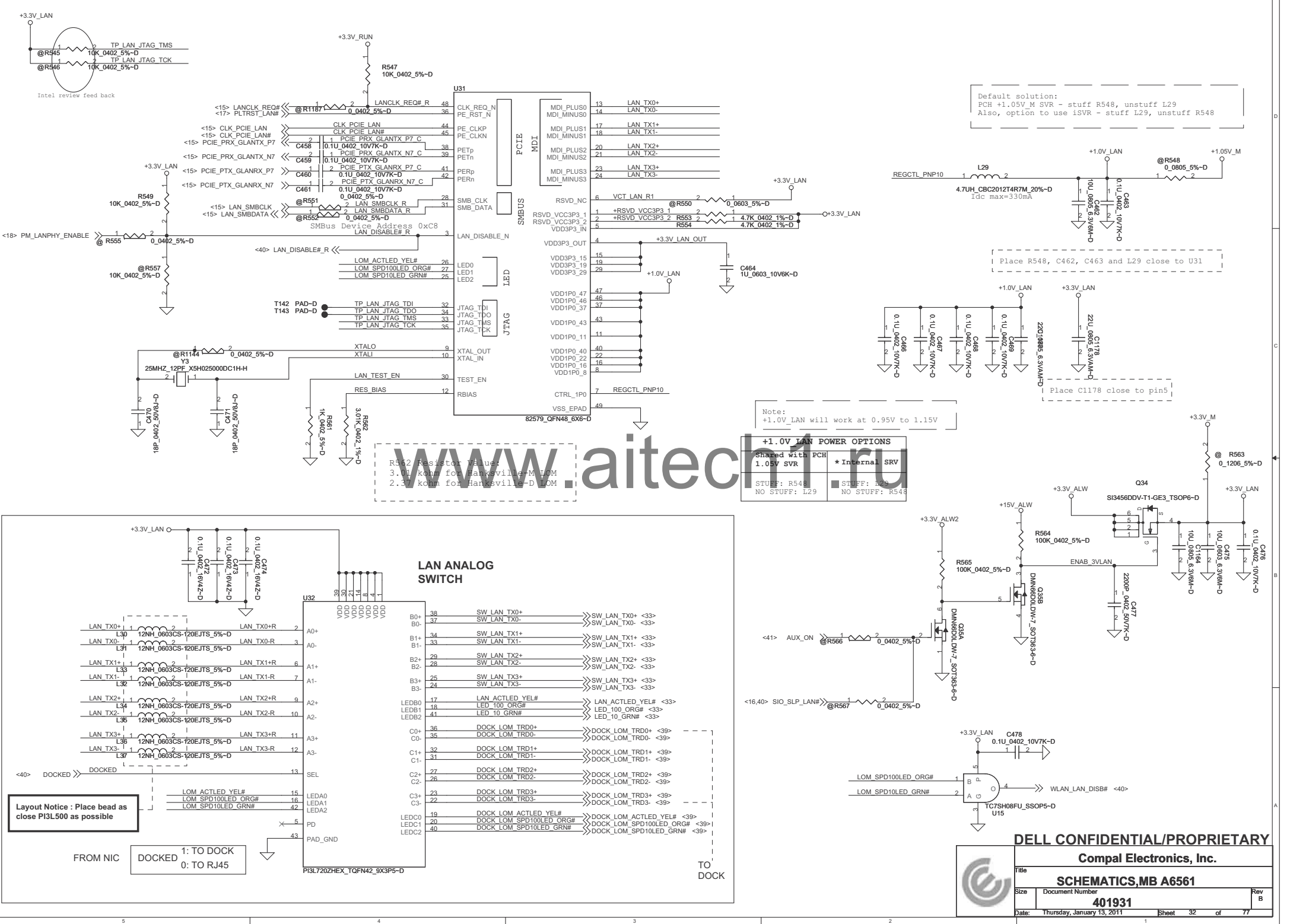
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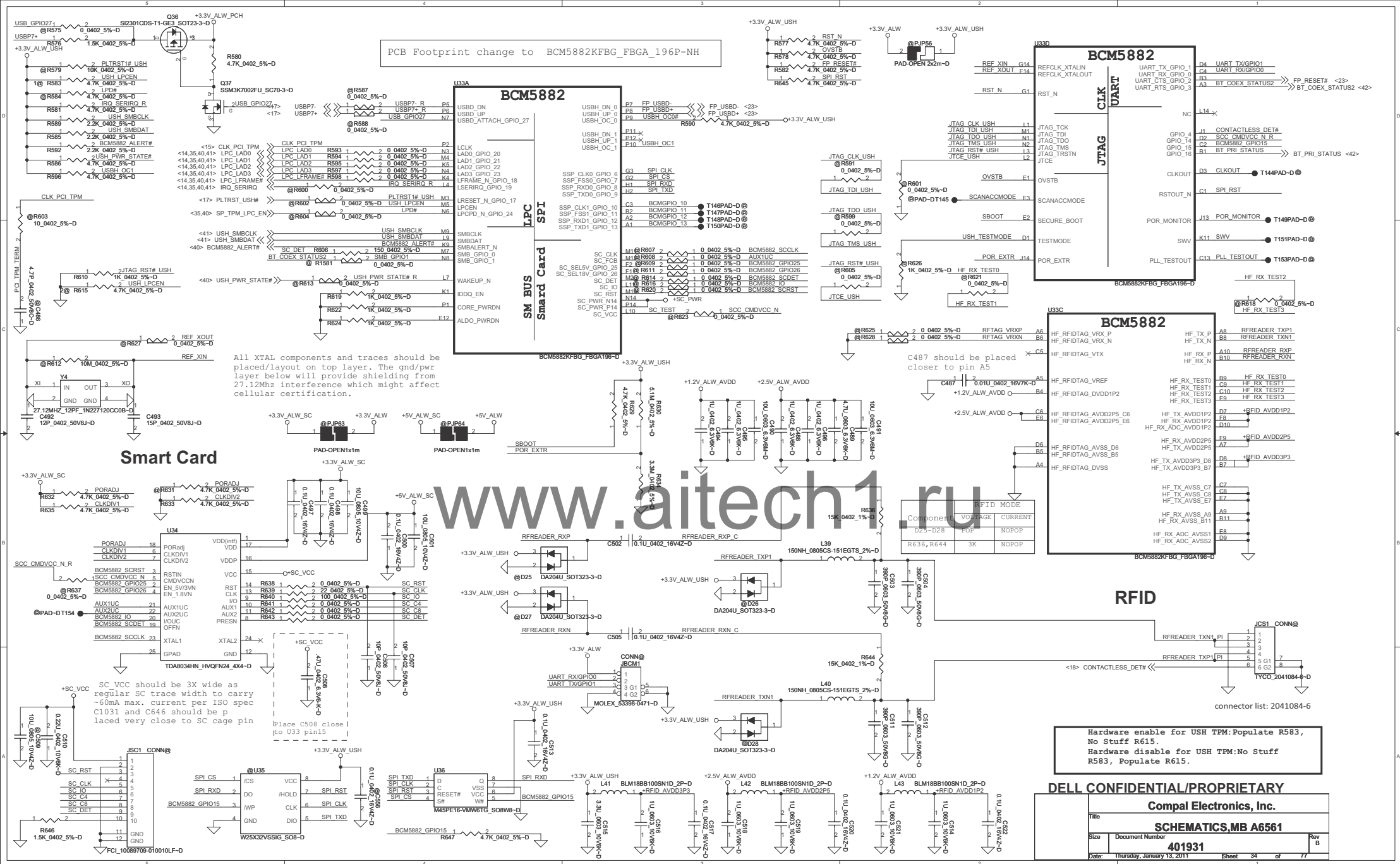
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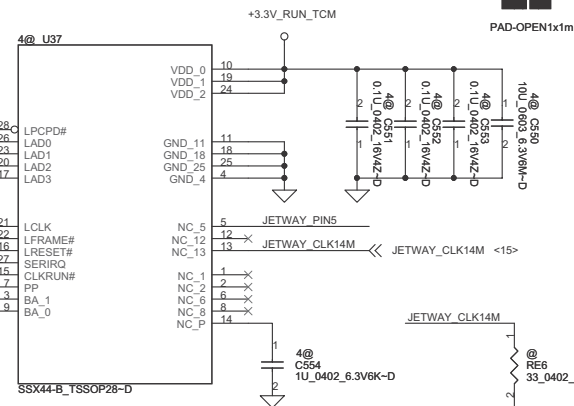
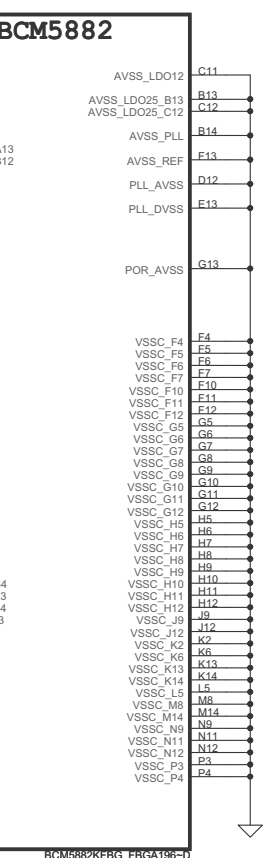
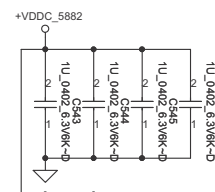
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TCM Vender	POP
NationZ	R660, R659, C554, C550
Jetway	C555, RH315

USH BCM5882 and China TCM Z8H172T Option				
PART/PIN	Ref Des	TCM Enable	TPM Enable	ALL TPM/TCM Disable
TCM circuit	All 4@	POP	@	@
USH_LPCEN	PU R583	@	POP	@
	PD R615	POP	@	@
SIO 5028 ->SP_TPM_LPC_EN	PU R772	@	@	@
PCH GPIO39 ->TPM_ID1	PU RH268	@	POP	POP
	PD RH271	POP	@	@
PCH GPIO38 ->TPM_ID0	PU RH267	@	POP	@
	PD RH270	POP	@	POP

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NOTE2:
If used OZ600RJ1-A R680 need change to 5.1K ohm 1%.
If used OZ600RJ1-B R680 need change to 191 ohm 1%.

NOTE3:
If used OZ600RJ1-A POP R679 JUMP +3.3V RUN.
If used OZ600RJ1-B CAN POP R679 or R678 JUMP +3.3V_RUN or +1.5V_RUN.
1.5V_RUN for POWER SAVING MODE.



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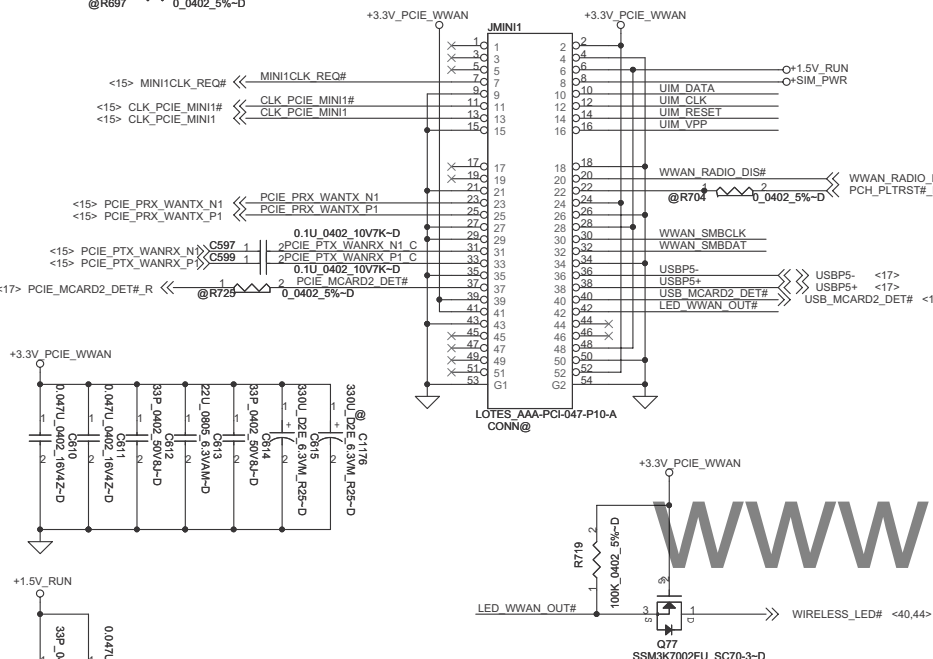


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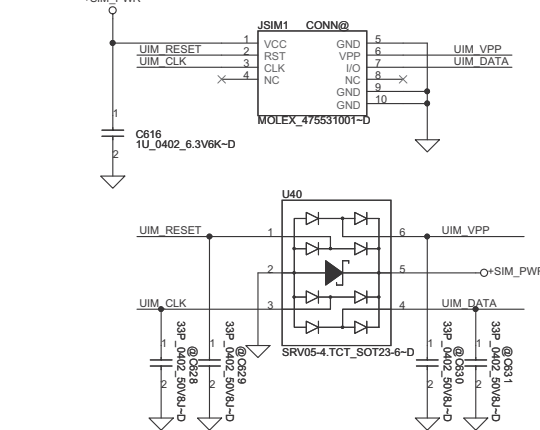
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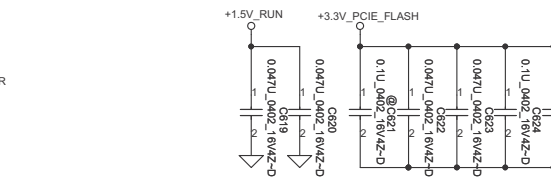
Mini WWAN/GPS/LTE/UWB H=5.2



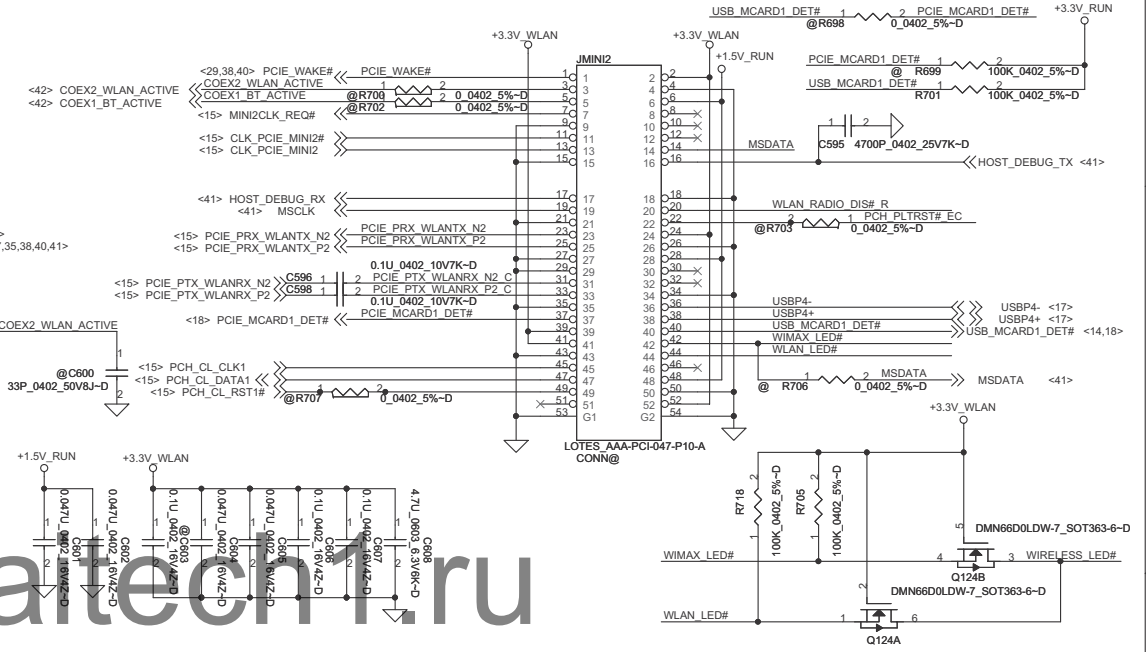
SIM Card Push-Push



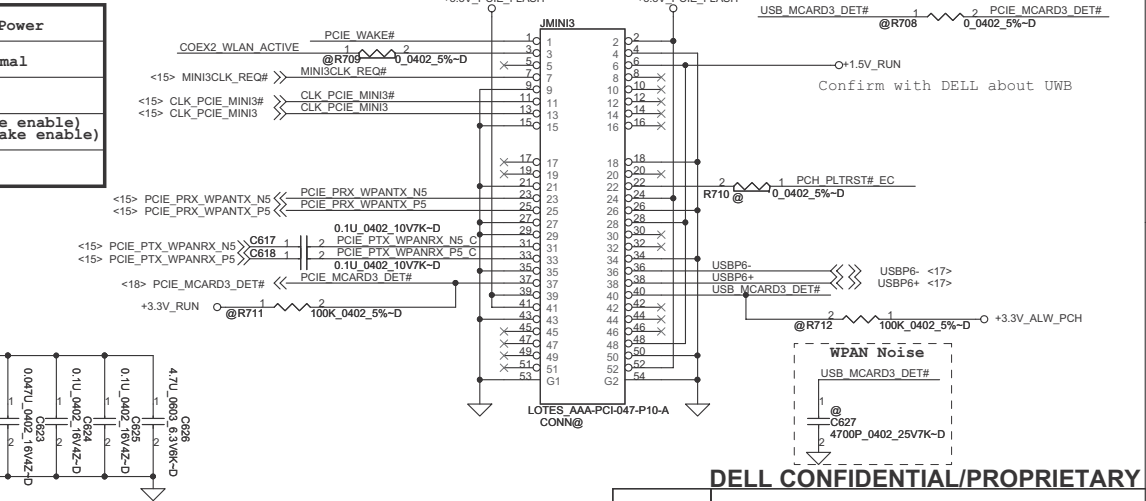
PWR Rail	Voltage Tolerance	Primary Power		Aux Power
		Peak	Normal	Normal
+3.3V	+ -9%	1000	750	
+3.3Vaux	+ -9%	330	250	250 (Wake enable) 5 (Not wake enable)
+1.5V	+ -5%	500	375	NA



Mini WLAN/WIMAX H=4



1/2 Minicard Flash Card H=4



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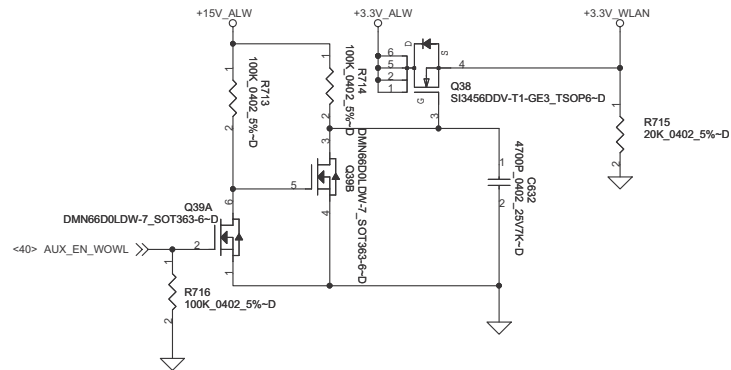
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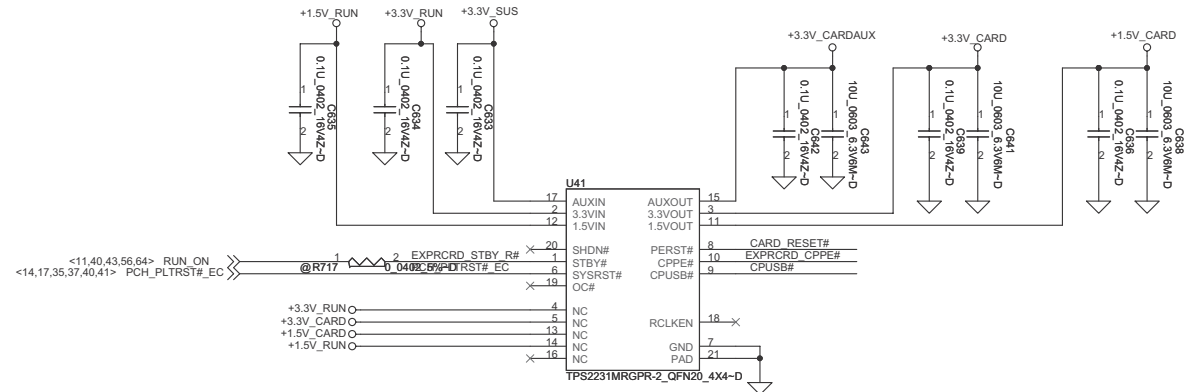
SCHEMATICS,MB A6561

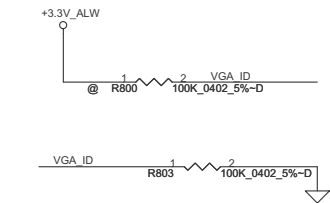
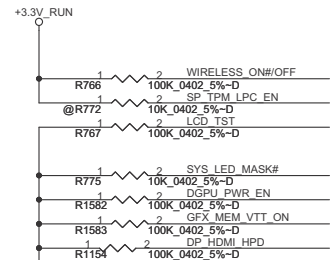
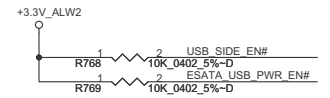
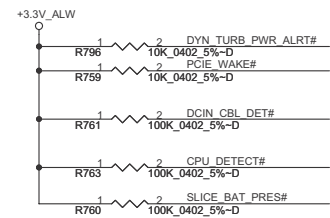
Size Document Number 401931
Date Thursday, January 13, 2011 Sheet 37 of 77

Power Control for Mini card1



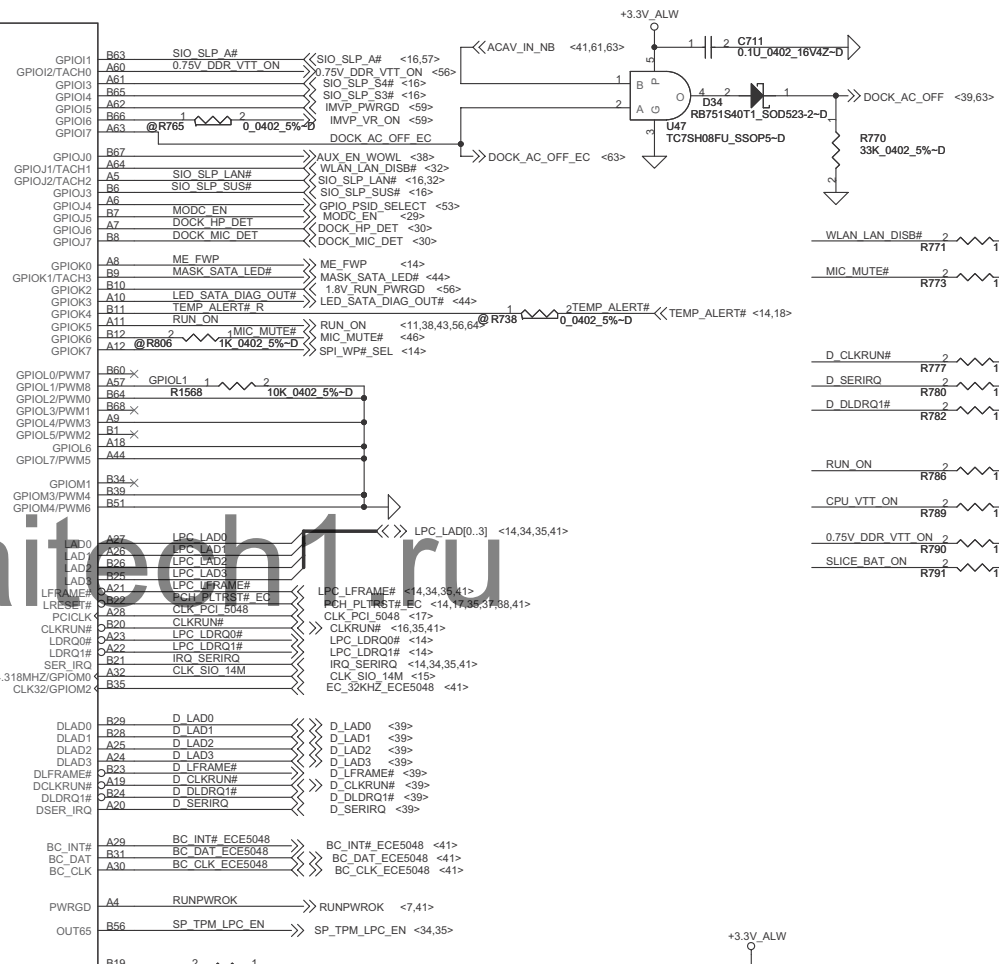
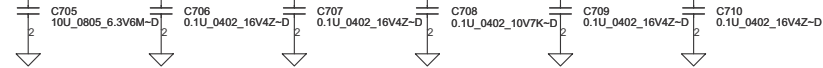
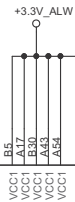
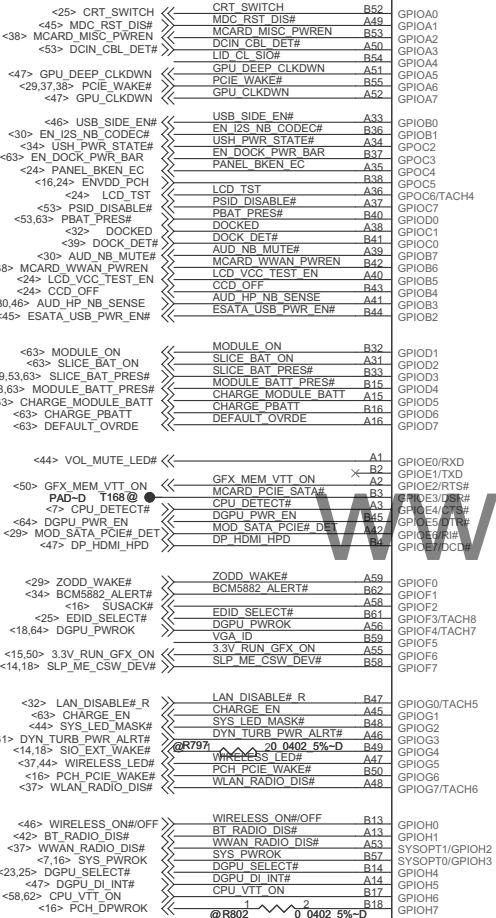
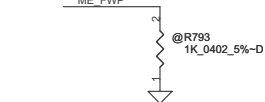
Express Card PWR S/W





	VGA_ID0
Discrete	0
UMA	1

ME_FWP PCH has internal 20K PD.
(suspend power rail)



DB Version 0.4
ECE5028-LZY_DQFN132_11X11-D

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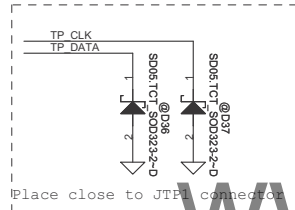
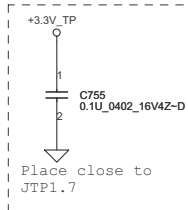
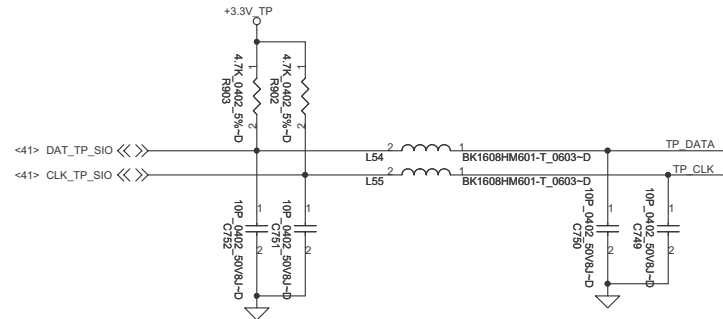
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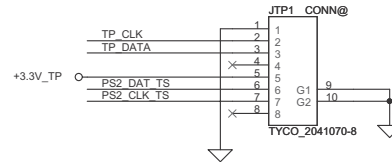
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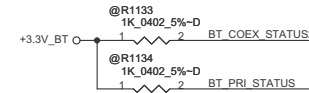
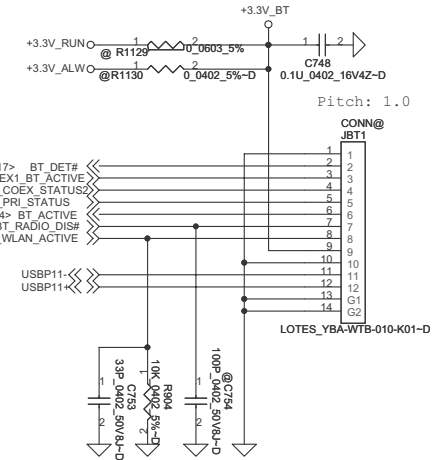
Touch Pad



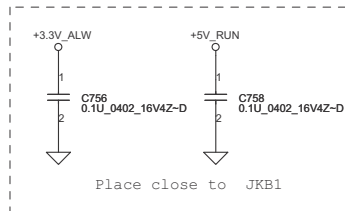
Pitch: 0.5



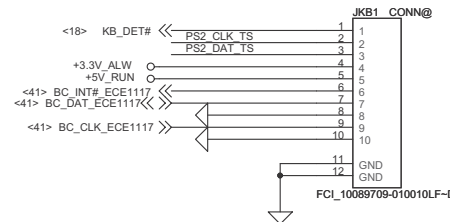
BlueTooth



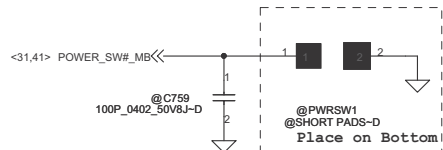
Keyboard



Pitch: 1.0



Power Switch for debug



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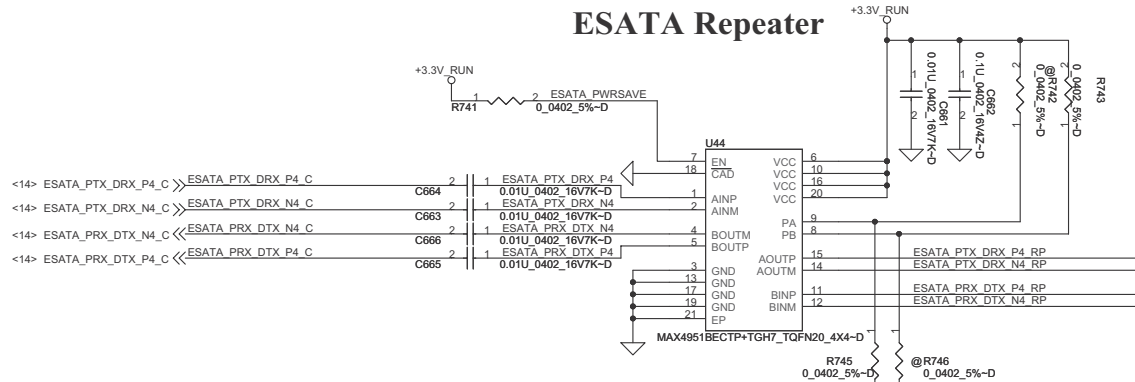
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Title			
SCHEMATICS,MB A6561			
Size	Document Number		Rev
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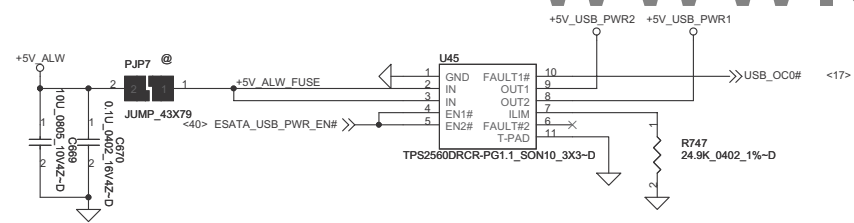
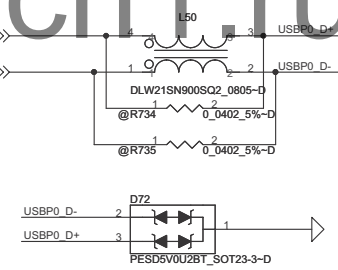
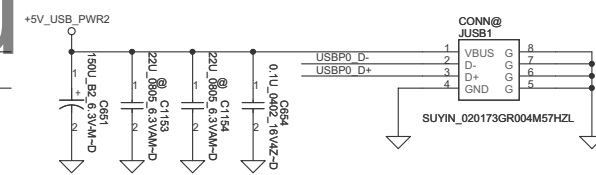
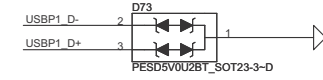
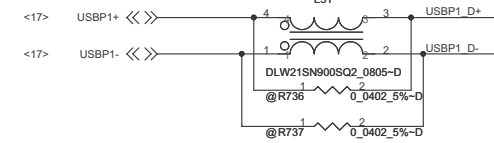
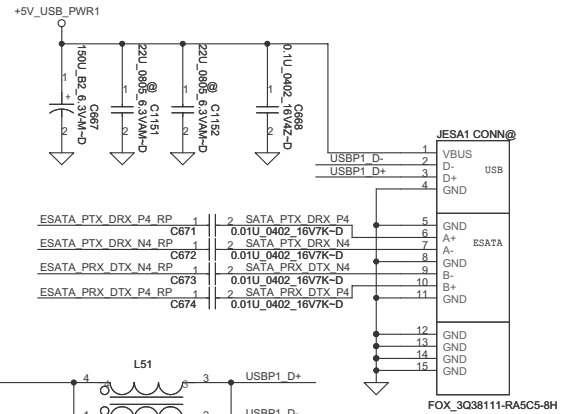
ESATA Repeater



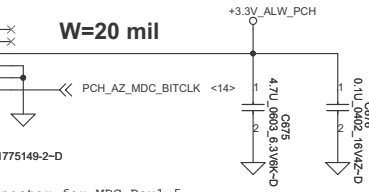
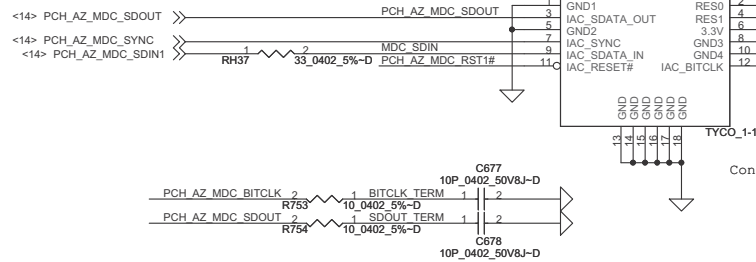
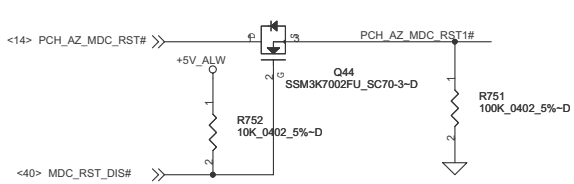
EN	CAD	STATUS
0	0	Low-Power Standby
0	1	Low-Power Standby
1	0	Active
1	1	Low-Power Standby

EN	PA	PB	CHANNEL A	CHANNEL B
0	X	X	Standby	Standby
1	0	0	Standard SATA	Standard SATA
1	1	0	Preemphasis	Standard SATA
1	0	1	Standard SATA	Preemphasis
1	1	1	Preemphasis	Preemphasis

Note: PA, PB, EN are internally pulled down to GND by 330kΩ resistors. CAD is internally pulled up to VCC by a 330kΩ resistor.
X = Don't care.



MDC CONN. H=5.5, Pitch=0.8



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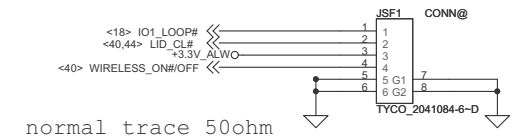
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power 20mil



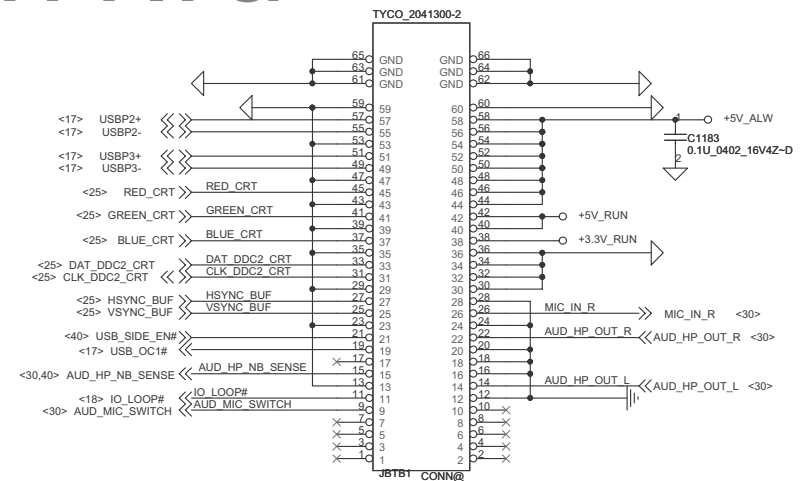
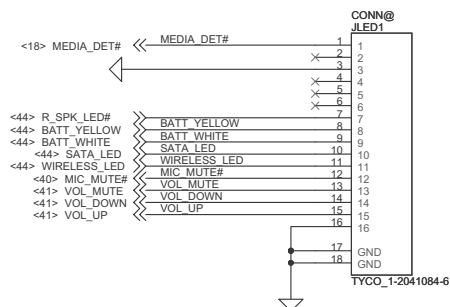
SNIFFER /Hall SENSOR IO BOARD

www.aitech1.ru

USBx2 /CRT/ AUDIO JACK IO BOARD

MEDIA BOARD

Default on,
WIRELESS_ON/OFF#:
LOW: ON
HIGH: OFF



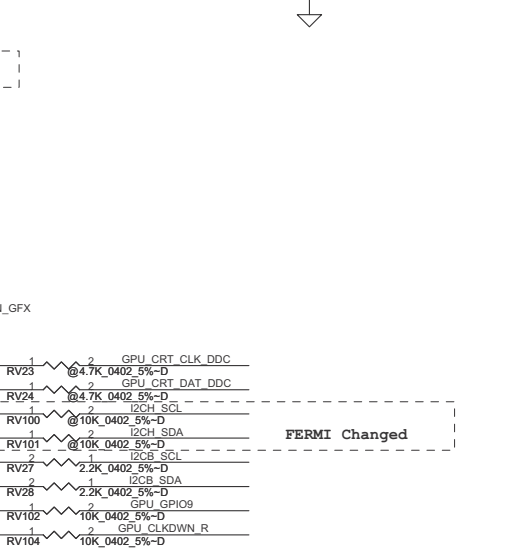
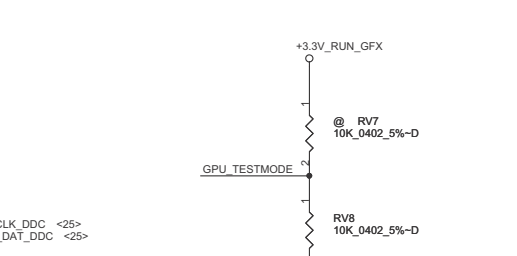
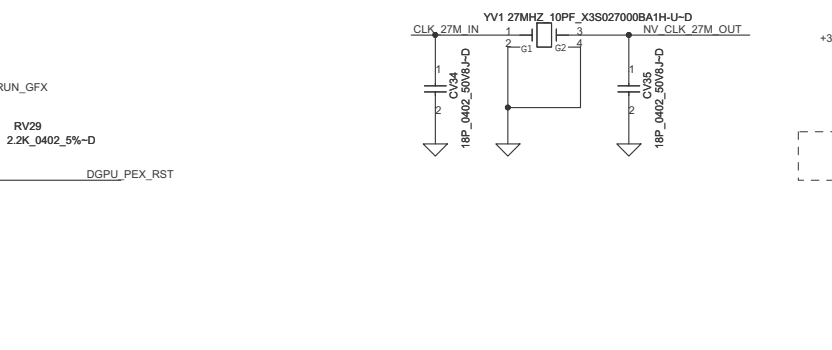
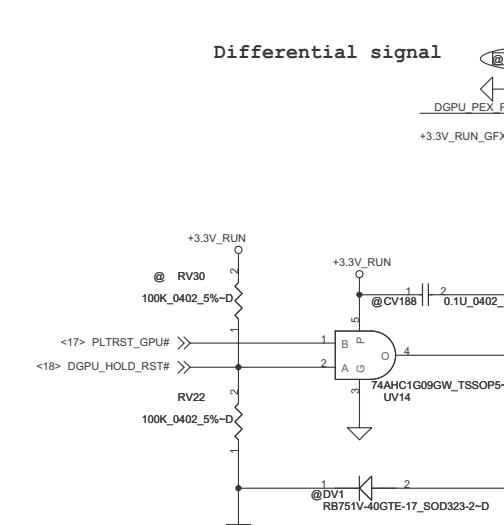
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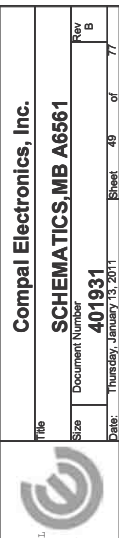
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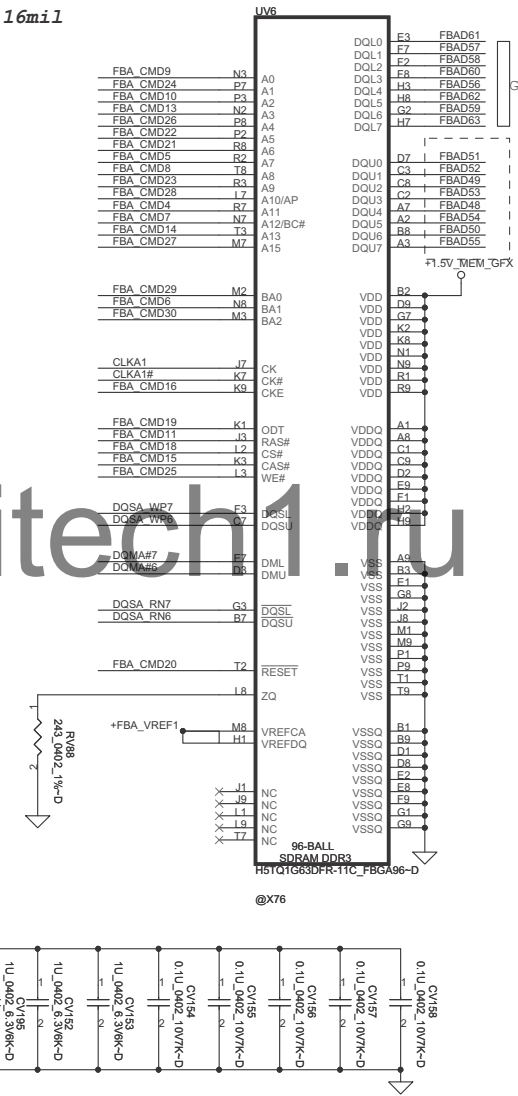
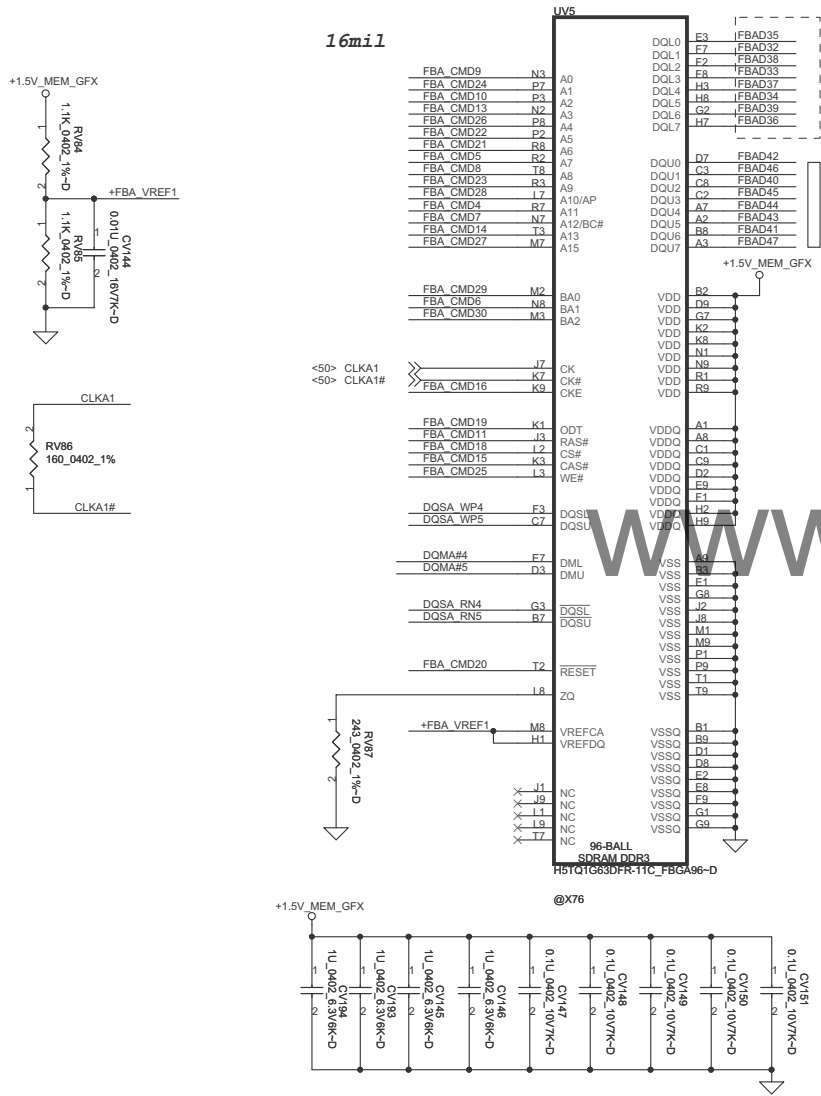


	DATA Bus	
Address	0..31	32..63
CMD0	ODT_L	
CMD1	CS1#_L	
CMD2	CS0#_L	
CMD3	CKE_L	
CMD4	A9	A11
CMD5	A6	A7
CMD6	A3	BA1
CMD7	A0	A12
CMD8	A8	A8
CMD9	A12	A0
CMD10	A1	A2
CMD11	RAS#	RAS#
CMD12	A13	A14
CMD13	BA1	A3
CMD14	A14	A13
CMD15	CAS#	CAS#
CMD16		CKE_H
CMD17		CS1#_H
CMD18		CS0#_H
CMD19		ODT_H
CMD20	RST	RST
CMD21	A7	A6
CMD22	A4	A5
CMD23	A11	A9
CMD24	A2	A1
CMD25	A10	WE#
CMD26	A5	A4
CMD27	BA2	A15
CMD28	WE#	A10
CMD29	BA0	BA0
CMD30	A15	BA2



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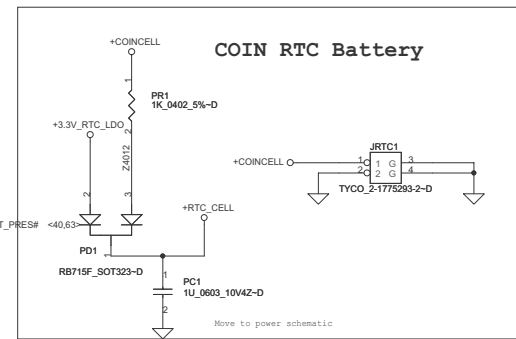
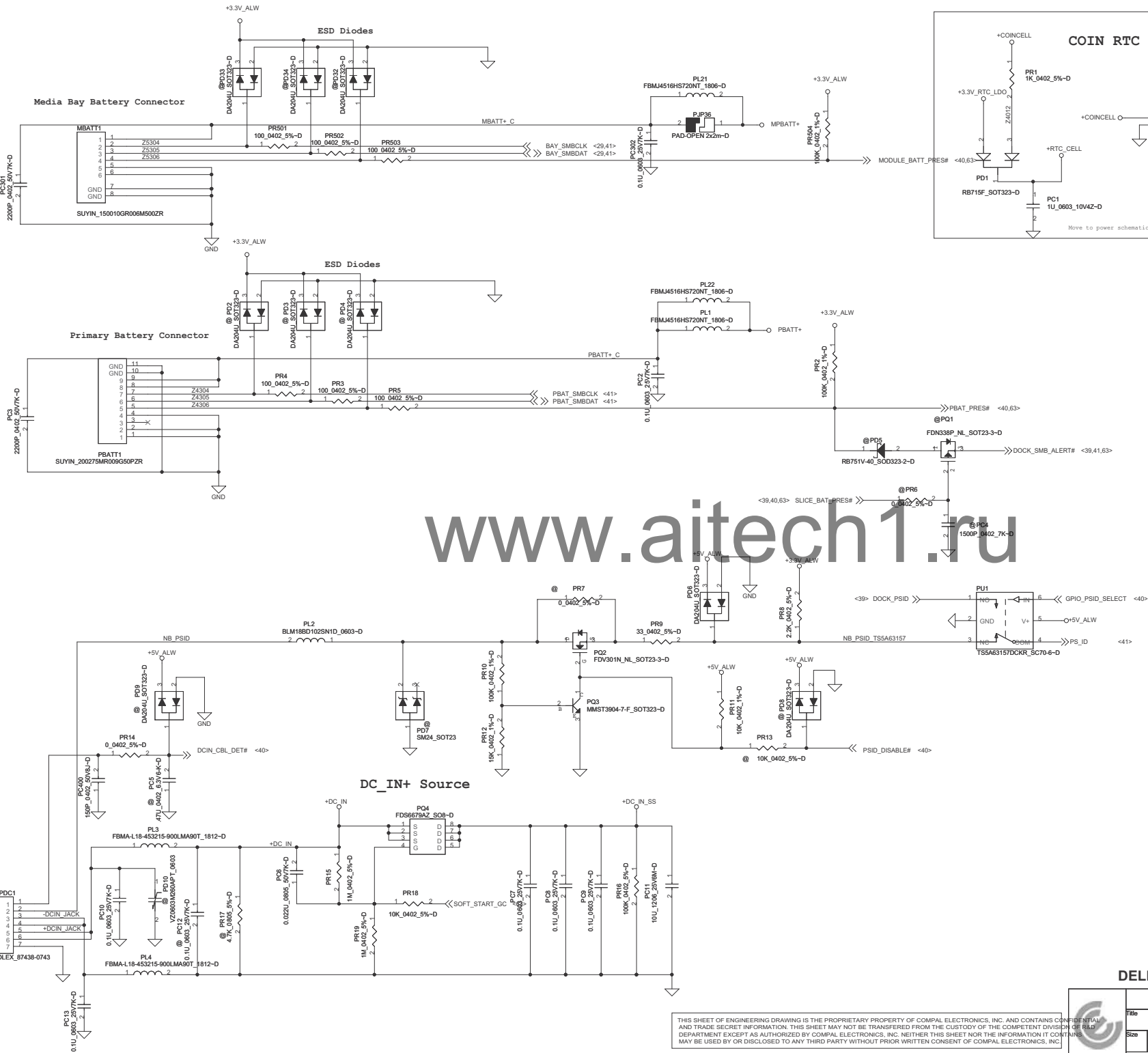
Memory Partition A - Upper 32 bits



Mode E - Mirror Mode Mapping

Address		DATA Bus	
CMD0	0..31	32..63	
CMD1	ODT_L		
CMD2	CS1#_L		
CMD3	CS0#_L		
CMD4	A9	A11	
CMD5	A6	A7	
CMD6	A3	BA1	
CMD7	A0	A12	
CMD8	A8	A8	
CMD9	A12	A0	
CMD10	A1	A2	
CMD11	RAS#	RAS#	
CMD12	A13	A14	
CMD13	BA1	A3	
CMD14	A14	A13	
CMD15	CAS#	CAS#	
CMD16		CKE_H	
CMD17		CS1#_H	
CMD18		CS0#_H	
CMD19		ODT_H	
CMD20	RST	RST	
CMD21	A7	A5	
CMD22	A4	A5	
CMD23	A11	A9	
CMD24	A2	A1	
CMD25	A10	WE#	
CMD26	A5	A4	
CMD27	BA2	A15	
CMD28	WE#	A10	
CMD29	BA0	BA0	
CMD30	A15	BA2	

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+3.3V_ALWP / +5V_ALWP / +5V_ALW2 / +15V_ALWP / +3.3V_RTC_LDO

5 Volt +/-5%
Thermal Design Current : 7.784A
Peak Current : 11.12A
OCP_MIN : 13.344A

Fsw = 400KHz

3.3 Volt +/-5%
Thermal Design Current : 4.708A
Peak current : 6.725A
OCP_MIN : 8.07A

Fsw = 300KHz

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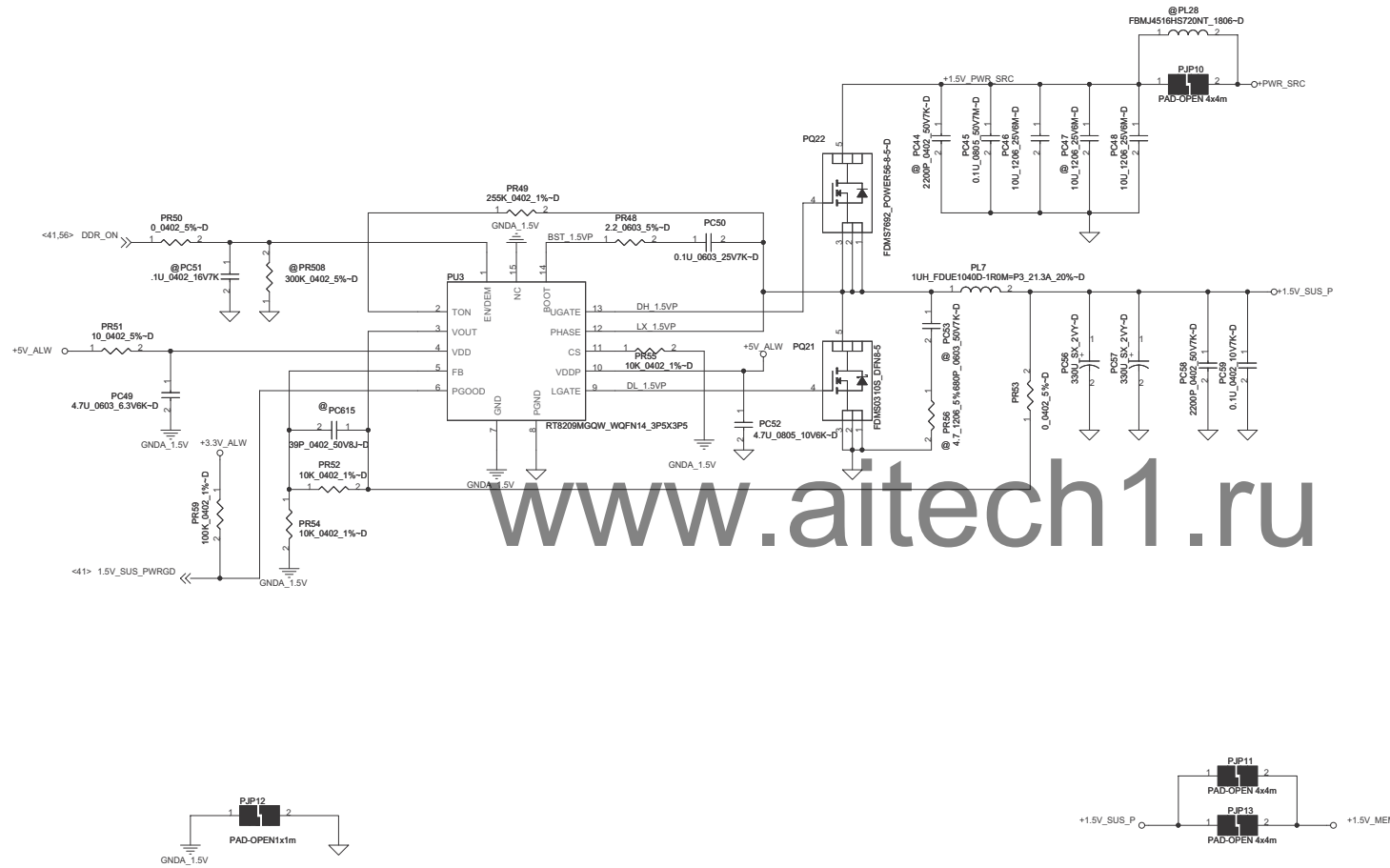
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+1.5V_SUS_P (RT8209B)

www.qdzbwx.com

1.5 Volt +/-5%
Thermal Design Current: 12.259A
Peak current: 17.513A
OCP_MIN: 21.016A



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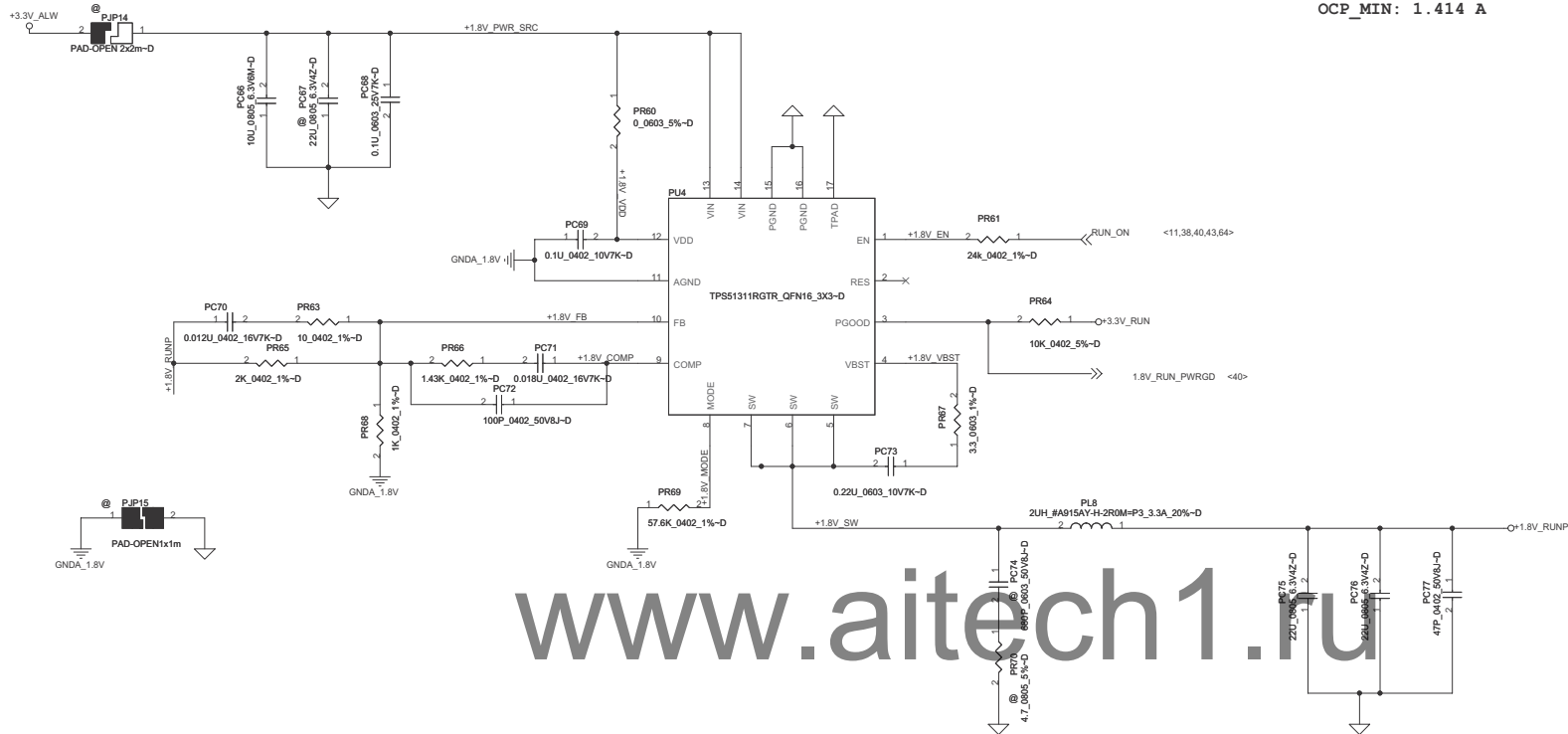
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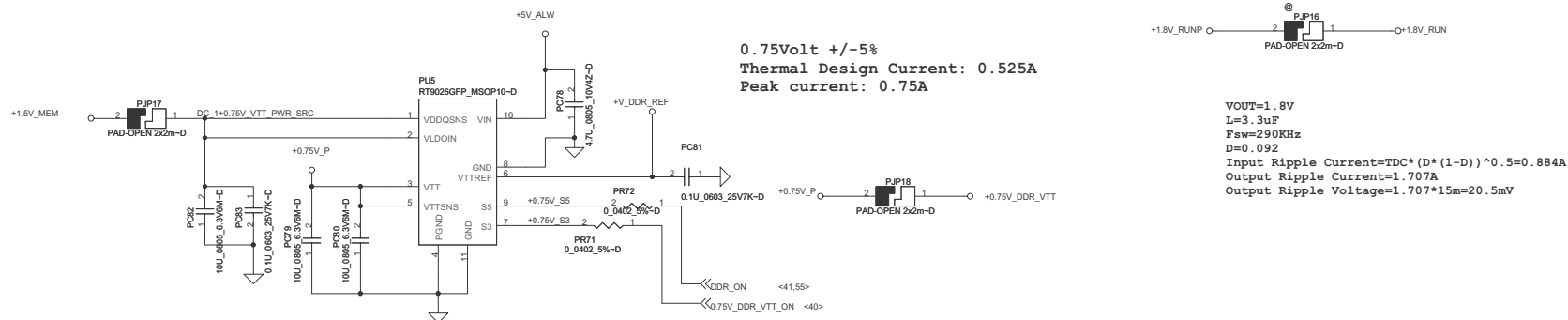
SCHEMATICS_MB A6561

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1.8 Volt +/-5%
Thermal Design Current: 0.824 A
Peak current: 1.178 A
OCP_MIN: 1.414 A



DDR3 Termination



```
VOUT=1.8V
L=3.3uF
Fsw=290KHz
D=0.092
Input Ripple Current=TDC*(D*(1-D))^0.5=0.884A
Output Ripple Current=1.707A
Output Ripple Voltage=1.707*15m=20.5mV
```

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Size

Number

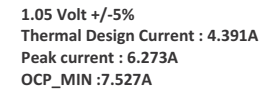
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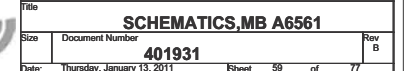
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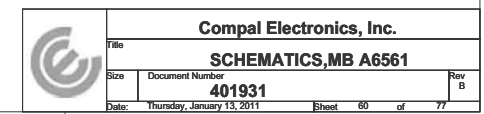
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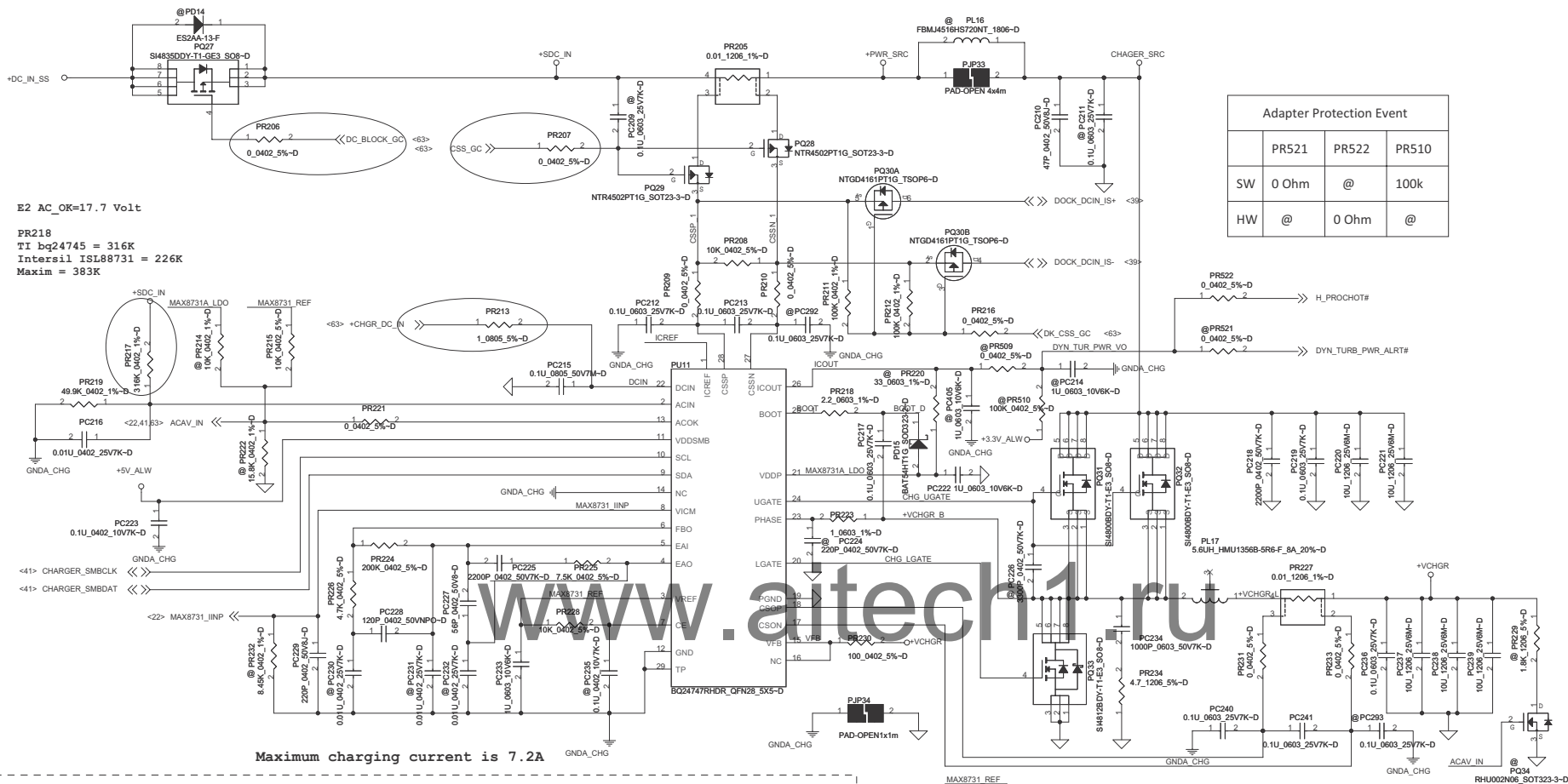
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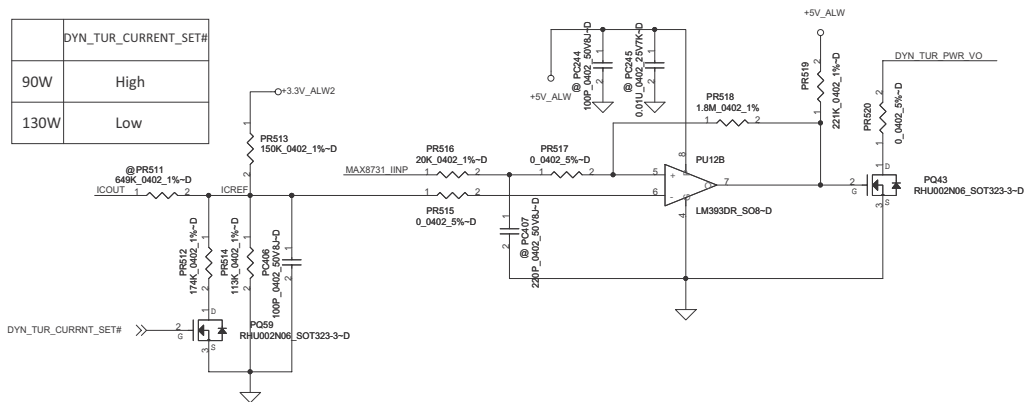
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Adapter Protection Event			
	PR521	PR522	PR510
SW	0 Ohm	@	100k
HW	@	0 Ohm	@

DYN_TUR_CURRENT_SET#	
90W	High
130W	Low



Adapter Protection Circuit fot Turbo Mode

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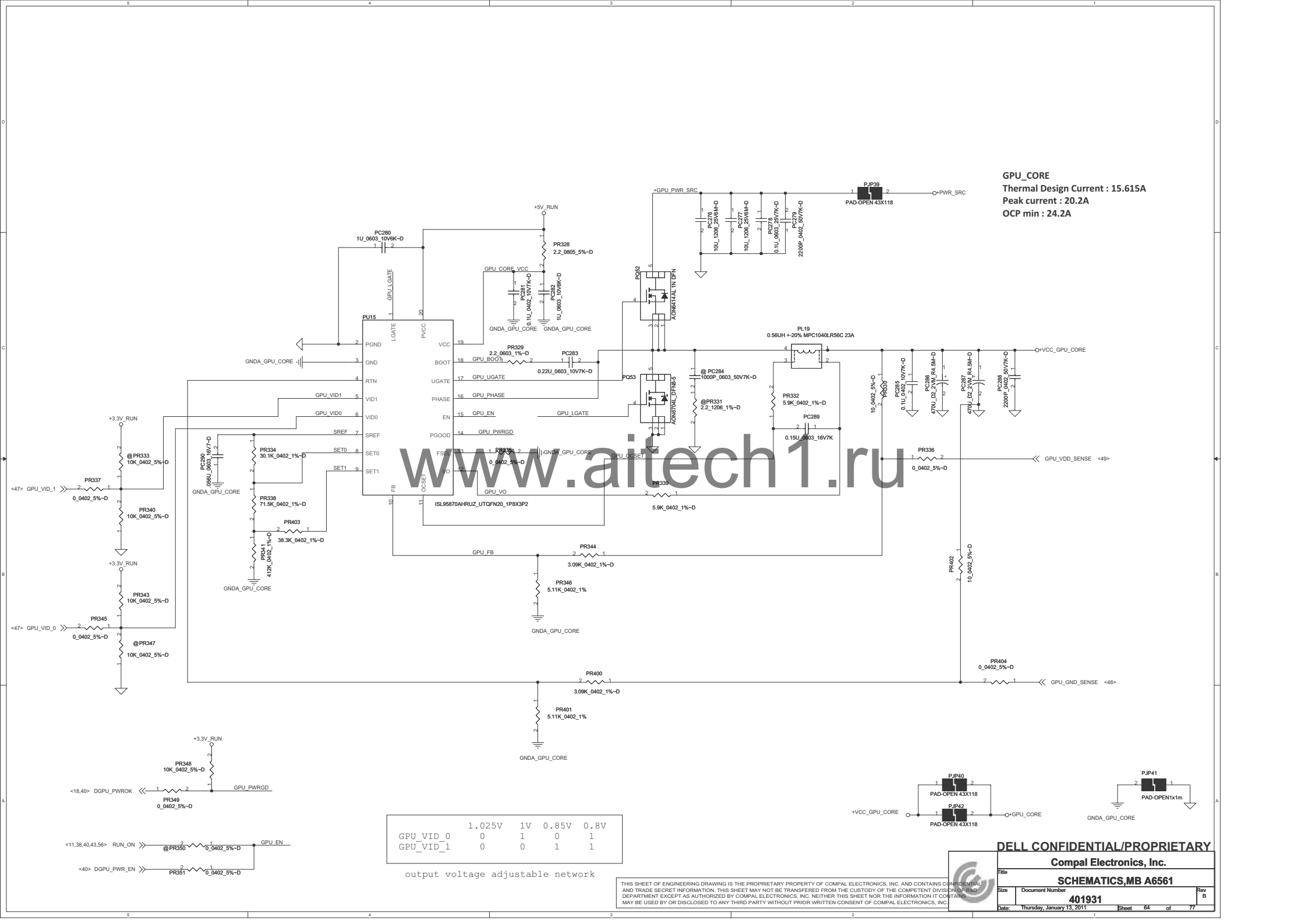
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GPU_CORE
Thermal Design Current : 15.615A
Peak current : 20.2A
OCP min : 24.2A

	1.025V	1V	0.85V	0.8V
GPU_VID_0	0	1	0	1
GPU_VID_1	0	0	1	1

output voltage adjustable network

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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	7	HW	6/15/2010	COMPAL	Boot issue	Change QC1 control from SUS_ON to RUN_ON_CPU1.5VS3#	X01
2	11	HW	6/15/2010	COMPAL	Modify net name	Change +0.8V_VCC_SA to +VCC_SA	X01
3	22,28,32,40,41,43,11,20,50,38	HW	6/15/2010	COMPAL	Follow PPM recommendation to change material	Change capacitors from 10uF_0805_10V_Y5V to 10uF_0805_6.3V_X5R: C305,C387,C462,C705,C728,C760,C764,C765,C768,C769, C772,CC135,CH58,CH73,CH80,CV124,CV126,CV185,CV187 Change capacitors from 10uF_0805_6.3V to 10uF_0603_6.3V: C475,C638,C641,C643 Change resistors to 0402 size: RC134, RH201,RH253,RH208,RH213 Delete RH192 and add PJP66	X01
4	14	HW	6/15/2010	COMPAL	De-pop PCH XDP	De-pop RH1,RH3~RH10,RH12~RH21,RH24,RH283~RH285,CH1	X01
5	14	HW	6/15/2010	COMPAL	Change HDA_SYNC topology	Add QH7 and RH37	X01
6	29	HW	6/15/2010	COMPAL	Change ODD connector from 13 pin to 31 pin	1. Change ODD connector to 31 pin, 2. Remove T157~T167,T169, U87~U89,C1168~C1170,R1181,R508. 3. Add Q123, Q76,R516,R514. 4. Change R510,R1177 power rail to +3.3V_ALW.	X01
8	18	HW	6/17/2010	INTEL	Follow Intel Design Guide Rev1.0	Change RH149 to 1k and RH150 to 4.7k	X01
9	22	HW	6/17/2010	COMPAL	Change EMC4002 to EMC4022	Change U9 to EMC4022, remove R392,R394 R866,R404,C279,R866, Reserve C277	X01
10	25	HW	6/17/2010	COMPAL	Change CRT SW to MAX14885	Change CRT SW to MAX14885 and add C1181,C1182,R1581,remove C325~C336	X01
11	26	HW	6/17/2010	COMPAL	Safety request	Add no stuff D4 and co-lay with F2, change F2 to 2A_8V	X01
12	45	HW	6/17/2010	COMPAL	Change E-SATA repeater to MAX4951BE	Chagne U44 to MAX4591BE and Reserve R1189~R1196 for bypass repeater	X01
13	30	HW	6/17/2010	COMPAL	Change Codec to ZB version.	Change U72 to ZB version as 92HD90B2X5NLGXZBX8 and stuff C962	X01
14	41	HW	6/17/2010	COMPAL	Board ID	Change R875 to 130K	X01
15	34	HW	6/17/2010	COMPAL	Change SI2301BDS to C version	Change Q36 to SI2301CDS	X01
16	34	HW	6/17/2010	BRCOM	Change RFID capacitors for more popular	Change C502,C505 from 1uF to 0.1uF	X01
17	18	HW	6/17/2010	COMPAL	Remove touch screen PAID pull down circuit	Remove RH241	X01
18	47	HW	6/17/2010	COMPAL	BIOS request	Reserve RV29, De-pop DV1, RV29 and pop U14	X01
19	46	HW	6/17/2010	COMPAL	ME request	Change the JBTB1 to TYCO_2041300-2 connector	X01
20	23	HW	6/17/2010	COMPAL	LVDS SW change to PI3LVD400ZFEX	1.Change U84, U85 to PI3LVD400ZFEX 2.Remove Q209,Q210, U91,U90	X01
21	41	HW	6/17/2010	COMPAL	Change BAY_SMBDAT and BAY_SMBCLK pull-up resistors to +3.3V_ALW	Change R854, R856 pull up power rail to +3.3V_ALW	X01

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22	11, 14, 41	HW	6/18/2010	COMPAL	EOL concern	Change CC176 to SGA00005H0L, change YH1, Y6 to SJ132P7KW1L	X01
23	42	HW	6/18/2010	COMPAL	Change connector	Change JKB1 to same as JSC1 Change JLED1 to TYCO_1-2041084-6	X01
24	42	HW	6/18/2010	COMPAL	Change TP pin definition	Reverse TP pin definition for PT	X01
25	40, 41	HW	6/18/2010	COMPAL	Add series resistor and pull up resistors on MIC_MUTE#, VOL_MUTE, VOL_UP, VOL_DOWN	Add R773, R806, R884, R886, R887, R1169, R1170, R1197	X01
26	24, 44	HW	6/18/2010	COMPAL	Correct net name for LED signal	Modify signal name BREATH BLUE LED to BREATH WHITE_LED and BREATH_BLUE_LED_SNIFF to BREATH_WHITE_LED_SNIFF	X01
27	40, 47	HW	6/21/2010	NVIDIA	Add HPD circuit to inform system for NV request	Add DV2, DV3, DV4, R1154 and use ECE5028 GPIOE7/DCD# as HPD signal to inform system	X01
28	32	HW	6/21/2010	INTEL	Remove useless resistors	Remove R556, R558, R559, R560 and short the pin1 and pin2 together	X01
29	24, 28, 30, 32, 38, 43, 50	HW	6/22/2010	COMPAL	Change part for Halogen free	Change Q18, Q27, Q30, Q34, Q38, Q40, Q42, Q49, Q54, Q58, QV5 to HF part	X01
30	10	HW	6/22/2010	COMPAL	To have better return path	De-pop CC130 and pop CC134	X01
31	43	HW	6/23/2010	COMPAL	Solution +1.5V_RUN voltage drop issue	Change Q59 from SI3456BDV to NTGS4141NT1G	X01
32	14	HW	6/23/2010	COMPAL	Add serial damping on SPI_CS0#, SPI_CS1# to avoid SPI_EA fail issue	Add serial damping resistor R935 47 ohm on SPI_CS0#, R936 22ohm on SPI_CS1#	X01
33	24	HW	6/25/2010	COMPAL	PT panel change touch screen pin definition	Change JTS1 pin definition for new TS pin define	X01
34	43	HW	6/25/2010	COMPAL	NTMS4107NR2G EOL	Change Q55 to NTMS4920NR2G	X01
35	14	HW	6/25/2010	COMPAL	Follow Intel XDP design	Change RH43, RH44, RH45 to 200 ohm	X01
36	24	HW	6/25/2010	COMPAL	Change LVDS connector to 40 pin	Change JLVDS1 to 40 pin as ACES_59003-0400C-001	X01
37	14, 41, 29	HW	7/1/2010	COMPAL	Modify Module Bay circuit	1.Remove R1181, R1182, R1189. 2.Change BAY_SMBUS, DEVICE_DET# pull up power rail from +3.3V_RUN to +3.3V_ALW. 3.Change net name ODD_DET# to PCH_SATA_MOD_EN#. 4.Add Q123, Q76, R513, R514, R515 for USB_SMI# circuit. 5.De-pop C627, R712	X01
38	24	HW	7/1/2010	COMPAL	Stuff PWM pull down resistor for PT solution	Pop R1137	X01
39	7	HW	7/1/2010	COMPAL	For support XDP device	De-pop RC9	X01
40	15, 18, 40, 41	HW	7/1/2010	COMPAL	Base on GPIO map to modify	1. Move SLP_ME_CSW_DEV# from GPIO45 to GPIO28, add MCARD_PCIE_SATA# on 5028 GPIOE3. 2. Remove RH238, change RH80 from 1k to 10k. 3. Change SLICE_BAT_PRES# pull up power rail from +3.3V_ALW2 to +3.3V_ALW. 4. Add R889	X01
41	24	HW	7/1/2010	COMPAL	PWM function	Remove R1139, R1140 and add D68, D69	X01
42	11	HW	7/1/2010	COMPAL	VCCSA VID circuit	Change VCCSA_VID_0 to VCCSA_VID_1 and pop RC138	X01

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43	22	HW	7/2/2010	COMPAL	Modify thermal diode for thermal request	Remove C268,C269, use DP1/DN1 for CPU,DP2/DN2 for GPU, DP3/DN3 for DIMM, DN5/DP5 for WWAM	X01
44	15,14,47	HW	7/8/2010	COMPAL	Meet Crystal EA chnage caps value.	1. CH18, CH19 change to 10P_0402_50V8J~D 2. CH2, CH3 change to 15P_0402_50V8J~D 3. CV34, CV35 change to 12P_0402_50V8J~D	X01
45	47	HW	7/8/2010	COMPAL	U14 power pin add 0.1uF bypass cap.	Add CV188 0.1uF CAP at U14.5 pin	X01
46	36	HW	7/12/2010	COMPAL	O2 suggest 1. add the damping resistors 33ohm on the (SD/MMCDAT0-7 and SD/MMCCMD) 2. change the resistor RE7 on the SD/MMC_CLK to 33ohm. 3. OZ600RJ1N rev.B PE_REXT change resistor	1. Add R1198~R1206 33 ohm 2. RE7 change to 33 ohm 3. R680 chnage to 191 ohm	X01
47	45,29	HW	7/12/2010	COMPAL	EMC request 1.Add 90 ohm common mode choke L50,L51 at USBP0+/- and USBP1+/- for USB R/W noise 2. Reserve 150pF bypass capacitor at ODD DEVICE_DET# 3.Add 220ohm Bead at DMIC_CLK for DMIC noise 4.Add 0 ohm at BIA_PWM_LVDS check UMA mode whether have PCI noise	1. L51,L50 change to POP, R734~R737 change to De POP. 2. Reserve CH7 150P 3. add LE2 220 ohm bead instead of R1106. 4. add RE9 0 ohm at BIA_PWM_LVDS	X01
48	24,45	HW	7/13/2010	COMPAL	PPM recommendation to change material	1.C300, C669 from 10U 16V Y5V 1206 change to 10U 10V Z Y5V 0805	X01
49	41	HW	7/13/2010	COMPAL	SMSC request 1.I2S_CLK, I2S_WS pull down resistors depopulated	R864 and R865 can be depopulated	X01
50	33	HW	7/15/2010	COMPAL	Hi-Pot EA Fail	JLOM1.14 change to NC, JLOM1.15 change to GND net,Remove C1165,C1166	X01
51	37,44	HW	7/15/2010	COMPAL	Modify LED circuit	Remove R1578,R1579,R1580,D42,D60,D61, add Q77,Q124,R705,R718,R719	X01
52	26	HW	7/15/2010	COMPAL	Meet HDMI EA, EMI	1.L19,L20,L21,L22 change to Populated 2.R470,R471,R468,R469,R462,R466,R451,R459 change to Depopulated	X01
53	37	HW	7/15/2010	COMPAL	MINI card CONN from H9.9 change to H9	JMINI1,JMINI2,JMINI3 change to LOTES_AAA-PCI-047-P10-A	X01
54	44	HW	7/15/2010	DELL	1.Remove MIC MUTE LED circuit, 2.Reserve SPK MUTE LED circuit	1.Remove the R1108,Q119,R1061,Q105 parts as MIC mute circuit 2.Reserve the R1109,Q119,Q102,R1059 parts as SPK mute circuit, Change Q119 to SSM3K7002FU	X01
55	14,17,18 40,41	HW	7/16/2010	COMPAL	Follow GPIO MAP	1.Remove R1567~R1577. 2.U46.B64,A9,A18,A44,B39,B51 connect to GND direct. 3.R796 Net rename to DYN_TURB_PWR_ALRT# then change to 10K value and pull up to +3.3V ALW power rail. 4.Add GPIO DYN_TUR_CURRNT_SET# TO U51.A35 and add R1171 10k pull up. 5.SIO_EXT_SMI# GPIO form PCH.GPIO1 change to PCH.GPIO14 and add RH51 10kohm Pull up 6.RH164 change to PCH_GPIO1 net. and remove RH254	X01
56	33	HW	7/19/2010	COMPAL	ME change reuquest	JLOM1 change to TYCO_2010019-3	X01

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57	36	HW	7/19/2010	COMPAL	OZ600RJ1 from A change to B version	U39 change to OZ600RJ1LN-B_QFN48	X01
58	20,43	HW	7/19/2010	COMPAL	Cost reduction as +3.3V_ALW_PCH and +5V_ALW_PCH power control circuit	1.Add PJP68 bypass JUMP for +5V_ALW to +5V_ALW_PCH 2.QH4,CH98,RH278 change to NON-POP 3.Add PJP67 bypass JUMP for +3.3V_ALW to +3.3V_ALW_PCH 4.Q51,R907,R905,C762,C760,R908,Q49 change to NON-POP	X01
59	24	HW	7/20/2010	COMPAL	Add BIA_PWM_GPU to control BIA_PWM_LVDS	D63 change to POP	X01
60	24	HW	7/20/2010	COMPAL	Meet LCD power sequence spec	R413 change to 470 ohm	X01
61	24	HW	7/20/2010	COMPAL	Corrent Touch screen pin define	Modify JTS1 pin define	X01
62	29	HW	7/20/2010	COMPAL	Q107 change to one channel	Q107 change to SSM3K7002FU_SC70-3~D	X01
63	47	HW	7/20/2010	NV	Follow NV request	Add @RV103,RV104, @RV20,@RV25,@RV26	X01
64	17,30,39	HW	7/20/2010	COMPAL	EMC team request	1.I2S_12MHZ add @RE13 2.I2S_BCLK add @RE10. 3.CLK_PCI_DOCK, RH103 change to 33ohm, R756 change to 33 ohm, C704 change to 12pf 4.DAI_BCLK# add@RE12,@CE9 5.DAI_12MHZ# add @RE11,@CE8	X01
65	26	HW	7/21/2010	COMPAL	Safety team request	Modify HDMI power circuit about D4,F2,R5 parts	X01
66	37	HW	7/21/2010	COMPAL	DF398754 Debug reserve	Reserve R725 0 ohm both PCIE_MCARD2_DET#R to PCIE_MCARD2_DET#	X01
67	36	HW	7/21/2010	COMPAL	Meet 1394 EA SPEC	R683,R684,R685,R686 from 56.2 change to 53.6 ohm	X01
68	36	HW	7/21/2010	COMPAL	Add MS card function	Modify U39 and JSD1 circuit	X01
69	30	HW	7/22/2010	COMPAL	EMI snubber and change Audio net name	1.Change net name from I2S_12MHZ to I2S_MCLK 2.Reserve R1587~R1590 part at INT_SPK bus	X01
70	41	HW	7/22/2010	COMPAL	New GPIO MAP	1.Pull up R943 to +3.3V_ALW on XFR_ID_BIT# of ECE5055-GPIO105 2.R712,R711,C627 change to de-pop	X01
71	40	HW	7/23/2010	COMPAL	TEMP_ALERT# Add 0 ohm jump between EC to PCH	Add R738 ohm at TEMP_ALERT#	X01
72	24,42	HW	7/24/2010	COMPAL	Follow GPIO map to add touch screen power down control circuit	Add TOUCH_SCREEN_PD#, Q125,Q32,R430,R431,C304,C306, and change JTCH1 pin 1,pin2 from +5V_RUN to +5V_TSP	X01
73	24	HW	7/26/2010	COMPAL	Reserve a 0 ohm option between +5V_RUN and +5V_TSP	Reserve R1001 0 ohm 0603 between +5V_RUN and +5V_TSP	X01
74	44	HW	7/26/2010	COMPAL	Due to BT_ACTIVE was folating pin, so, add 100 Kohm pull down	Add R944 100K ohm for BT_ACTIVE pull down	X01
75	49	HW	7/28/2010	NV	Follow NV suggestion to modify BOM	De-pop CV184, and change CV183 to 1uF,CV182 to 4.7uF, CV109 to 470pF,CV110 to 4700pF, LV8 to 100nH	X01

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76	24	HW	9/06/2010	COMPAL	In order to use the HF part.	Q21 change SB000009K0L to SB000009K1L	X02
77	14,18	HW	9/06/2010	Intel	Follow Intel request	Add RH52 and RH53.	X02
78	38,45	HW	9/15/2010	COMPAL	For the part consist issue.	L49,L50,L51 change SM01002080L to SM070001E0L	X02
79	45	HW	9/17/2010	COMPAL	Remove Bypass ESATA Repeater schematic, because Gen1 EA fail when Bypass ESATA Repeater.	Remove R1189~R1196.	X02
80	15,36	HW	9/17/2010	H.ELE.	YH2's CL value can't match cd & cg value. Y5's value too low that frequency shift of PCB board.	CH18 & CH19 change from 10P to 22P, C591 & C592 change from 10P to 6.8P.	X02
81	47,48,49 50,51,52	HW	9/21/2010	DELL	Macallan DIS performance request.	UV change from N12M to N12P.	X02
82	30	HW	9/23/2010	IDT	MIC detect issue.	U72 change version from SA00003ZZ1L(ZB) to SA00003ZZ2L(YA).	X02
83	47	HW	9/23/2010	COMPAL	De-pop pull up resistors	De-pop RV23,RV24	X02
84	18	HW	9/23/2010	Intel	Follow Intel design guide Rev1.2	Change RH149 to 2.2k and RH150 to 0 ohm	X02
85	32	HW	9/23/2011	Intel	Intel request	U31 change version from WG82579LM QMWM A2 to WG82579LM QNGP C0.	X02
86	15,32	HW	9/24/2011	H.ELE.	modify item 80 YH2's CL value can't match cd & cg value.	CH18 & CH19 change from 22P to 10P and YH2 change from CL=18pF to CL=12pF. C470 & C471 change from 33P to 18P and Y3 change from CL=18pF to CL=12pF.	X02
87	34	HW	9/24/2011	Broadcom	Broadcom request	Add decoupling cap C556 for U35 on layout.	X02
88	24	HW	9/24/2011	COMPAL	The PWM can not function correct.	R1137 change from 100K to 10K.	X02
89	41	HW	9/24/2011	EPSON	The frequency skew of Y6 is too big in Normal temperature.	C741 & C743 change from 33P to 39P,	X02
90	36	HW	9/25/2011	COMPAL	Correct the 53.6 ohm into L end part number.	Change the R683,R684,R685,R686 to SD00000HE8L	X02
91	46	HW	9/25/2011	COMPAL	Add bypass cap at IO board connector of MB side.	Add bypass cap C1183 at +5V_ALW.	X02
92	38	HW	9/25/2011	COMPAL	Correct the Express Card PWR S/W into L end part number.	Change the U41 to SA00001SL2L.	X02
							X03

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93	47,48,49,51,52	HW	9/27/2010	NVIDIA	NVIDIA request.	1. CV160~CV162 change to 1uF 2. Change CV41/42/43/50/51 to 0.022u 3. Change CV40/58/59/60 to 0.1u 4. No stuff CV58/44 on DSC 5. Change CV181 to 22uF_0805 6. Change +SP_PLLVDD to +PLLVDD and remove CV182,CV183,CV184,CV115,LV8 7. Change LV3 to SM01000BE0L 8. Change CV34/35 to 18pF 9. Reserve 1x1mm jumper and contact to PEX_SVDD_3V3. 10. CV90 placement under GPU 11. Change CV80 to 4.7u. 12. Add 2pcs of 1uF per VRAM 13. Change RV81,RV86 to 160_1% 14. Add 10K pull-down to UV1.J5 15. Add 40.2K_1% pull down on UV1.T6	X02
94	36	HW	9/28/2010	O2Micro	O2Micro request.	1. Move C582 to +MMI_1394 VCCH and close to either one pin 28 or pin 33. 2. Move C581 to +MMI_PE_VDDH and close to pin1. 3. Add a 0.01uF capacitor on +MMI_PE_VDDH and close to pin1.	X02
95	30,31	HW	9/30/2010	IDT	To solve pop noise and detect issue	Add U6,Q33,Q46,D70,D71,R425,R33,R38,R424,R161,R352,R1088,C967,C307,C308 Q107 change from SB00000960L(3pin) to SB00000DH0L(6pin)	X02
96	30	HW	9/30/2010	COMPAL	EMC request	Add bypass cap C1185~C1188	X02
97	14,09	HW	10/04/2010	Intel	Following Intel DG ver1.5	1. Add RH31 pull down resistor. 2. RC96,RC97 no stuff	X02
98	34	HW	10/04/2010	Broadcom	Broadcom request(enhancement current amount)	L39 & L40 change from SHI00005Y0L(0603 size) to SHI0000CH0L(0805 size rate current is 400mA).	X02
99	11	HW	10/04/2010	COMPAL	Change QC5 VGS MAX rating from 12V to 20V	Change QC5 from SB52302028L to SB00000HK0L	X02
100	24,26,47	HW	10/04/2010	COMPAL	Change RB751V to HF part	Change D53,D63~D69,DV1~DV4 to SCS00004L0L	X02
101	7,18,41	HW	10/04/2010	COMPAL	For cost saving	Remove RH159,RH261	X02
102	30	HW	10/06/2010	COMPAL	1. Sync-up with Macallan 14" 2. EMC request	1. Remove R1587~R1590, C1185~C1188, change R1183~R1186 to L91~L94 2. Change Audio signal's diode from 4 of 2pins(SD05.TCT) to 2 of 3pins (PESD5V0U2BT SCA00000T0L)	X03
103	38	HW	10/06/2010	COMPAL	In order to enable Express Card PWR S/W 2nd source vendor "GMT" to act.	Add connection of pin4,pin5,pin13 and pin14 to power net.	X03
104	26	HW	10/06/2010	COMPAL	Follow safety request	Pop F2 and de-pop R5	X03
105	53,14	HW	10/06/2010	COMPAL	Remove PAID function of RTC	1. JRTC1 change from 3pin to 2pin(SP02000CA0L) and remove detect pin 2. UH4.C36 & RH355.2 rename from RTC_DET# to PCH_GPIO33	X03

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106	29	HW	10/06/2010	COMPAL	For power saving	Increase JSATA2 detect pin R1177 from 1k to 100kohm	X03
107	46	HW	10/07/2010	COMPAL	For NB board space consider.	Remove page46 two block MIC detect schematic to IO/B.	X03
108	28	HW	10/07/2010	COMPAL	For cost saving	De-pop the R505,Q28,R500,R499,C393,C394,R504 parts.	X03
109	32	HW	10/07/2010	COMPAL	Based on IEEE Return Loss EA fail	L30~L37 change from SHI0000400L(22NH) to SHI00005I0L(12NH)	X03
110	28	HW	10/07/2010	COMPAL	Based on support SSD HDD	Add +3.3V_RUN on JSATA1 pin8,pin9,pin10	X03
111	47	HW	10/07/2010	COMPAL	solve system can't boot in UMA only mode.	correct from U14 to UV14 and change the PN to SA00003Y00L. pop RV29.	X03
112	30,32,40 42	HW	10/07/2010	COMPAL	GPIO MAP update at 1-Oct-10	1. Add U15, C478 that defect RJ45 cable insert or not if plug in then close WLAN power. 2. 5048 GPIOB7 rename from AUD_NB_MUTE to AUD_NB_MUTE#	X03
113	18,30	HW	10/08/2010	COMPAL	Remove PAID function of speaker	1. JSPK1 change from 6pin to 4pin(LTCX002V50L) that remove detect pin 2. UH4.D40 & RH269.2 rename from SPEAKER_DET# to GPIO17	X03
114	48,49	HW	10/08/2010	nVIDIA	Follow nVIDIA suggest	1.Move CV74 to contact +3.3V_RUN_VDD33 not +3.3V_RUN_GFX 2.RV41 change to 4.99K 1% and RV99 change to 20K 1%.	X03
115	44	HW	10/11/2010	COMPAL	LED brightness test result	change R957 to 1K, R955, R941, R949, R939, R934 to 4.7K	X03
116	41	HW	10/11/2010	COMPAL	BORAD ID	change R875 to 62K.	X03
117	17	HW	10/11/2010	Intel	Follow Intel check list Rev1.2	Add CRH332	X03
118	31,41	HW	10/12/2010	DELL	DELL DM Dennis has confirmed.	No stuff "Latitude On" button of SW2,R877,C740	X03
119	24,45	HW	10/13/2010	COMPAL	EMC request(for cost saving)	1.UE1,UE2,U13,U86 change from PRTR5V0U2X(SOT143-4) (4pin) to PESD5V0U2BT(SOT23-3) (3pin) SCA00000T0L. 2.Diode for UE1,UE2 shall be added, not reserved. 3.Rename UE1 to D73,UE2 to D72,U86 to D74,U13 to D75	X03
120	28	HW	10/13/2010	COMPAL	Follow 14"	PJP71 size change to 1X1	X03
121	7	HW	10/14/2010	COMPAL	UC1.4 is OD pin,so remove pull down R.	Remove RC11	X03
122	22,47,48 49	HW	10/14/2010	nVIDIA	Follow nVIDIA suggest	1.Change R1111 to 10K for power saving. 2.No stuff of CV188,RV50,CV159 and stuff of RV56,RV41,RV99,CV58 3.Change RV51 to 45.3K, CV109 & CV110 to 0.1uF	X03
123	30	HW	10/14/2010	COMPAL	Audio team Paul's agree the EMI solution.	Stuff of C973~C976	X03
124	28	HW	10/15/2010	COMPAL	MikeCC suggest	Stuff of R505,C394,R504	X03
125	14,18	HW	10/19/2010	COMPAL	Follow Intel debug port DG	Connect PCH_GPIO15 to PCH_XDP_FN16	X03
126	30	HW	10/19/2010	COMPAL	Change Mic detect to external detect	Remove R161 and add C1165	X03
127	51,52	HW	10/25/2010	DELL	DELL request	Change VRAM from 128Mx16 to 64Mx16	X03

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128	30	HW	11/10/2010	COMPAL	Modify Mic detect circuit	1.Move C1180 to +VREFOUT_R 2.No stuff C967,R352,R1088	X04
129	14~21	HW	11/10/2010	COMPAL	Change PCH stepping	Change UH4 to B2 stepping	X04
130	18	HW	11/16/2010	COMPAL	Follow check list Rev1.0	Change RH177 from 1k to 10k	X04
131	15	HW	11/16/2010	COMPAL	To fix ME issue (transition fail S3/Moff->S3/M3)	De-pop RH296,RH297; pop QH5,RH302,RH303	X04
132	47	HW	11/19/2010	NV	Solve HDMI audio issue	De-pop RV41, change RV97 to 34.8K and stuff it	X04
133	47	HW	11/19/2010	NV	Chagne Device ID to 0x1056	De-pop RV51,change RV57 to 34.8k and stuff De-pop RV60, change RV54 to 10k and stuff it, change RV52 to 4.99k	X04
134	47,48, 49,50	HW	11/19/2010	NV	Change GPU to QS sample	Change UV1 to N12P-NS-S-A1	X04
135	28	HW	11/19/2010	Intel	Follow Intel CRB design	Change R501,R502 to 10k	X04
136	38	HW	11/19/2010	COMPAL	To fix soldering issue	Change express card connector JEXP1 to TAISOL 5-421005002000-9	X04
137	45	HW	11/19/2010	COMPAL	To fix pericom ESATA Repeater that PA internal pull high.	Stuff R745 that channel A from preemphasis to standard SATA of Pericom.	X04
138	47	HW	11/26/2010	COMPAL	Correct the DGPU_HOLD_RST# behavior.	Reserve Pull-up resistor RV30 to DGPU_HOLD_RST#,but de-pop RV30.	X05
139	14	HW	11/26/2010	COMPAL	Remove Resistor between +3.3V_ALW_PCH_JTAG and +3.3V_ALW_PCH.	Remove RH288.	X05
140	41	HW	12/06/2010	COMPAL	Follow INTEL DG1.5 RSMRST# timing cicuit	Just add RSMRST# circuit for backup. but de-pop.	X05
141	18	HW	12/07/2010	COMPAL	GPIO17 for interior MIC and exterior MIC detect function.	Reserve pull-down resistor RH273 to GPIO17,but De-pop RH273.	X05
142	41	HW	01/07/2011	COMPAL	BOARD ID.	Change R875 from 62k to 33k.	A00
143	35	HW	01/07/2011	COMPAL	PWM and backlight timing issue.	Reserve 74AHC125 circuit for BIA_PWM_GPU, but de-pop.	A00
144	35	HW	01/07/2011	COMPAL	Modify TPM/TCM configuration table.	Update USH BCM5882 and China TCM Z8H172T Option table.	A00
145	ALL	HW	01/11/2011	COMPAL	For cost saving	Change 119pcs 0402 0 ohm resistors and 3pcs 0603 0 ohm footprint to new footprint which is short pin1 and pin2 .	A00

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1	54	+3V/+5V	7/5	Compal	+3.3V phase node over Mosfet Vds rating	Change PQ6 from SI4128 to AO4466L. Change PQ8 from SI4134 to AO4712L.	
2	62	0.8V_VCCSA	7/5	Intersil	VCCSA spike issue	Remove PR264 and add PR410 connect PR249.1 to do PD. Remove VCCSA_VID_0 net to connect PR249.1 and change net name to VCCSA_VID_1 Change PR250 from 34K to 113K Change PR256 from 0 to 140K Change PR261 and 265 from 2.49K to 0 ohm. Change PD resistor PR266 and PR410 to 1K. Depop PR249, PR260 and PR267 Change PR259 from 274K to 47.5K	
3	53	+DCIN	7/19	Compal	Add 150pF bypass capacitor for PCI noise	Add PC400 to connect PR14.1 and gnd	
4	55	+1.5V_SUS	7/19	Compal	Vendor will not support this part	Change PC56 and PC57 to 330U/9m/2V (SGA20331E0L) from 330U/9m/2.5V (SGA19331D1L)	
5	53	+DCIN	7/19	Compal	PL3 and PL4 current rating is not enough for 130W adapter	Change PL3 and PL4 to FBMA-L18-453215-900LMA90T (SM01002078L) from FBMJ4516HS720NT(SM010009C8L)	
6	53	+DCIN	7/19	Compal	PL1 current rating is not enough for 9cell (3.0Ah 1C) discharge current	Change PL1 to FBMJ4516HS720NT(SM010009C8L) from FBMA-L18-453215-900LMA90T (SM01002078L) Add PL22 FBMJ4516HS720NT(SM010009C8L) Take off PJP45	
7	53	+DCIN	7/19	Compal	PR16 down size to 0402 from 0805	Change PR16 to 100k/0402 (SD02810038L) from 100k/0805 (SD01510038L)	
8	54	+3V/+5V	7/19	Compal	PC24 down size to 0603 from 0805	Change PC24 to 4.7u/6.3V/0603 (SE107475K8L) from 4.7u/6.3V/0805 (SE093475K8L)	
9	55	+1.5V_SUS	7/19	Richtek	Reserve 300K PD to avoid VR turn on when EN/DEM is floating.	Add PR508 to do PD from PU3 pin1	
10	61	Charger	7/19	Compal	solve leakage issue	Change PD14 to ES2AA-13-F (SC100005A0L) from SBR3A40SA-13_SMA2 (SC100003J00)	
11	63	Selector	7/19	Compal	solve leakage issue	Change PD16 to ES2AA-13-F (SC100005A0L) from SBR3A40SA-13_SMA2 (SC100003J00)	
12	58	+1.05V_VIT	7/19	Compal	Remove PC147 for ME Interfere	Remove PC147	
13	62	0.8V_VCCSA	7/19	Compal	VCCSA phase node over Mosfet Vds rating	Change PQ35 from SI4128 to AO4466L. Change PQ36 from SI4172 to AO4712L.	
14	59	VCORE	7/19	MAXIN	Fine tuning VCORE Load Line	Change PR140 to 11.8k(SD03411828L) from 12.6k(SD00000AJ8L)	
15	59	VCORE	7/19	MAXIN	Reserve 33nF cap parallel with PC136 to fine tuning VCORE transient	Add PC401 33nF/16V/X7R/0402(SE076333K8L)	
16	59	VCORE	7/19	MAXIN	Fine tuning VGFX Load Line	Change PR157 to 8.2k(SD00000418L) from 8.66k(SD03486618L)	
17	60	VGFX	7/19	MAXIN	Add 33nF cap parallel with PC208 to fine tuning VGFX transient	Add PC402 33nF/16V/X7R/0402(SE076333K8L)	

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18	61	Charger	7/21	Compal	Reserve adapter protection circuit for turbo mode	Change PU11 pin1 net name to ICREF from GNDA_CHG Change PU11 pin26 net name to ICOUT from VCC Reserve PR511, PR512, PR513, PR514, PC406, PQ59, PR515, PR516, PR517, PC407 PC244, PC245, PR518, PR519, PR520, PQ43, PC405, PR509, PR510	X01
19	61	Charger	7/21	Compal	PQ27 body diode can handle surge current when adapter plug in so depop PD14	Depop PD14 SBR3A40SA (SC100003J00)	X01
20	59	VCORE	7/23	MAXIN	For Pass2 VCORE & VGFX OCP setup	Change PR126 & PR127 to 165K from 150K Change PR134 & PR135 to 105K from 100K	X01
21	59/60	VCORE/VGFX	7/23	MAXIN	Setting change for ICC version change	Change PR118 to 1 ohm from 2 ohm Change PR119 to 1 ohm from 2 ohm	X01
22	61	Charger	7/28	TI	Pop adapter protection component for turbo mode with TI solution	Pop PR513 100k (SD03410038L) Pop PR514 78.7k (SD03478728L) Pop PR512 115k (SD03411538L) Pop PR511 1.87M () Pop PQ59 RHU002N06 (SB50206008L) Pop PR510 100K (SD02810038L) Pop PC406 100P (SE071101J8L)	
23	57	+1.05VM	10/18	TI	Fine tune OCP setting	Change PR83 to 22k (SD03422028L) from 10k (SD03410028L)	
24	63	Selector	10/18	Compal	Change parts to HF parts	Change PQ39 and PQ44 SI4835DDY-T1-GE3 (SB00000FF1L) from SI4835DDY-T1-E3 (SB00000FF0L)	
25	61	charger	10/18	Compal	Fine tune adapter protection circuit to reserve B PROCH014	Depop PR814	
26	57	+1.05VM	10/18	Compal	22u/1206/6.3V COS issue	Change PC98 ~ PC105 to 22u/0805 (SE00000110L) from 22u/1206 (SE077226M8L)	
27	58	+1.05VTT	10/18	Compal	22u/1206/6.3V COS issue	Change PC123 ~ PC125, PC121, PC127, PC120, PC129 and PC130 to 22u/0805 (SE00000110L) from 22u/1206 (SE077226M8L) Change PC122 and PC126 to 47u/0805 (SE00000G60L) from 22u/1206 (SE077226M8L)	
28	53	DCIN	10/18	Compal	6 ~ 7mA leakage current in slice	Change PR2 and PR504 to 100K (SD02810038L) from 10K (SD03410028L)	
29	64	GPU_Core	10/18	nVidia	Fix output voltage to 0.9V for nVidia ES sample	Depop PR337 and PR345 0 Ohm (SD02800008L) Depop PR347 10K (SD02810028L) Pop PR343 10K (SD02810028L)	
30	64	GPU_Core	10/18	Compal	Change OCP setting for new nVidia chip	Change PR332 and PR339 to 5.9k (SD03459018L) from 4.22k (SD03442218L)	
31	62	VCCSA	10/18	Compal	Fine tune VCCSA OCP setting for 2nd and 3rd source choke	Change PR247 and PR262 to 12.7k (SD03412728L) from 11.5k (SD03411528L)	
32	64	GPU_Core	11/11	nVidia	Change VID setting for new nVidia chip. Default set 1V.	Depop PR347 10K (SD02810028L) Pop PR343 10K (SD02810028L) Change PR344 and PR400 to 3.09k (SD00000J38L) from 3.57k (SD03435718L) Change PR341 to 412k (SD00000678L) from 402k (SD034402380) Change PR403 to 38.3k (SD03438328L) from 200k (SD03420038L) Change PR338 to 71.5k (SD03471528L) from 0 Ohm (SD02800008L) Change PR334 to 30.1k () from 23.7k (SD03423728L)	

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33	63	Selector	11/11	Compal	Fine tune main and media battery switching to slice battery transient time	Change PC270 and PC265 to 0.22uF (SE000005Z8L) from 1uF (SE00000698L)	
34	61	Charger	11/11	Compal	Change adapter protection circuit trip point. (Adapter rated current + 0.75A)	Change PR512 to 107k (SD03410738L) from 115k (SD03411538L) Change PR511 to 649K (SD03464938L) from 1.87M (SD000000WN0L) Change PR514 to 80.6K (SD03480628L) from 78.7k (SD03478728L)	
35	61	Charger	11/11	Compal	Change adapter protection event to HW from SW	Pop PR522 0 Ohm (SD02800008L) Depop PR521 0 Ohm (SD02800008L) Depop PR510 100k Ohm (SD02810038L)	
36	60	VGFX_core	12/08	Compal	Fine tune the GFX initial voltage to solve offset	Change PR119 to 0 ohm (SD01300008L) from 1 ohm (SD014100B8L)	
37	59	VCORE	12/08	Compal	Fine tuning VCORE Load Line	Change PR140 to 12.4k(SD00000AJ8L) from 11.8k(SD03411828L)	
38	61	Charger	12/10	Compal	H_PROCHOT# can not pull high issue with external circuit at DC mode	Change PR513.1 net nam to +3.3V ALW2 from MAX8731_REF Change PQ59.3, PR514.2 and PC406.2 net nam to PGND from GAND_CHG	
39	61	Charger	12/10	Compal	H_PROCHOT# pull low level can not meet Intel SPEC with HW solution at AC mode	Depop PR511 (SD03464938L) Change PR512 to 174k (SD03417438L) from 107k (SD03410738L) Change PR513 to 150k (SD03415038L) from 100k (SD03410038L) Change PR514 to 113k (SD03411338L) from 80.6K (SD03480628L) Pop PR515, PR517, PR520 0 Ohm (SD02800008L) Pop PQ49 RH0002N08 (SB50206008L) Pop PR519 221K (SD00000HX8L) Pop PR518 1.8M (SD00000K180) Pop PR516 20K (SD03420028L) Depop PR509 (SD02800008L)	
40	59	VCORE	12/10	Compal	Fine tune the GFX Load Line	Change PR157 to 8.06K ohm (SD03480618L) from 8.2K ohm (SD00000418L)	

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